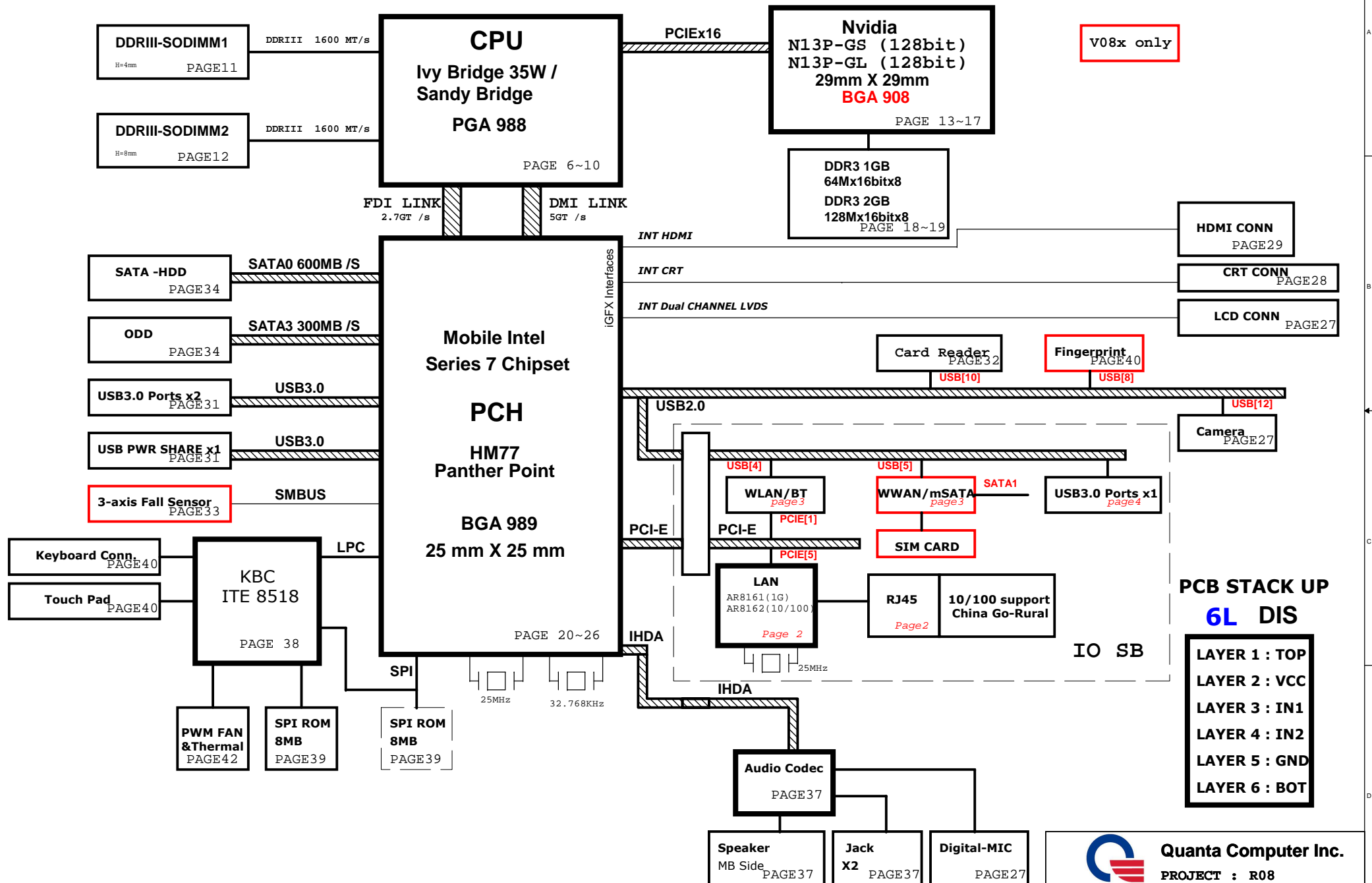
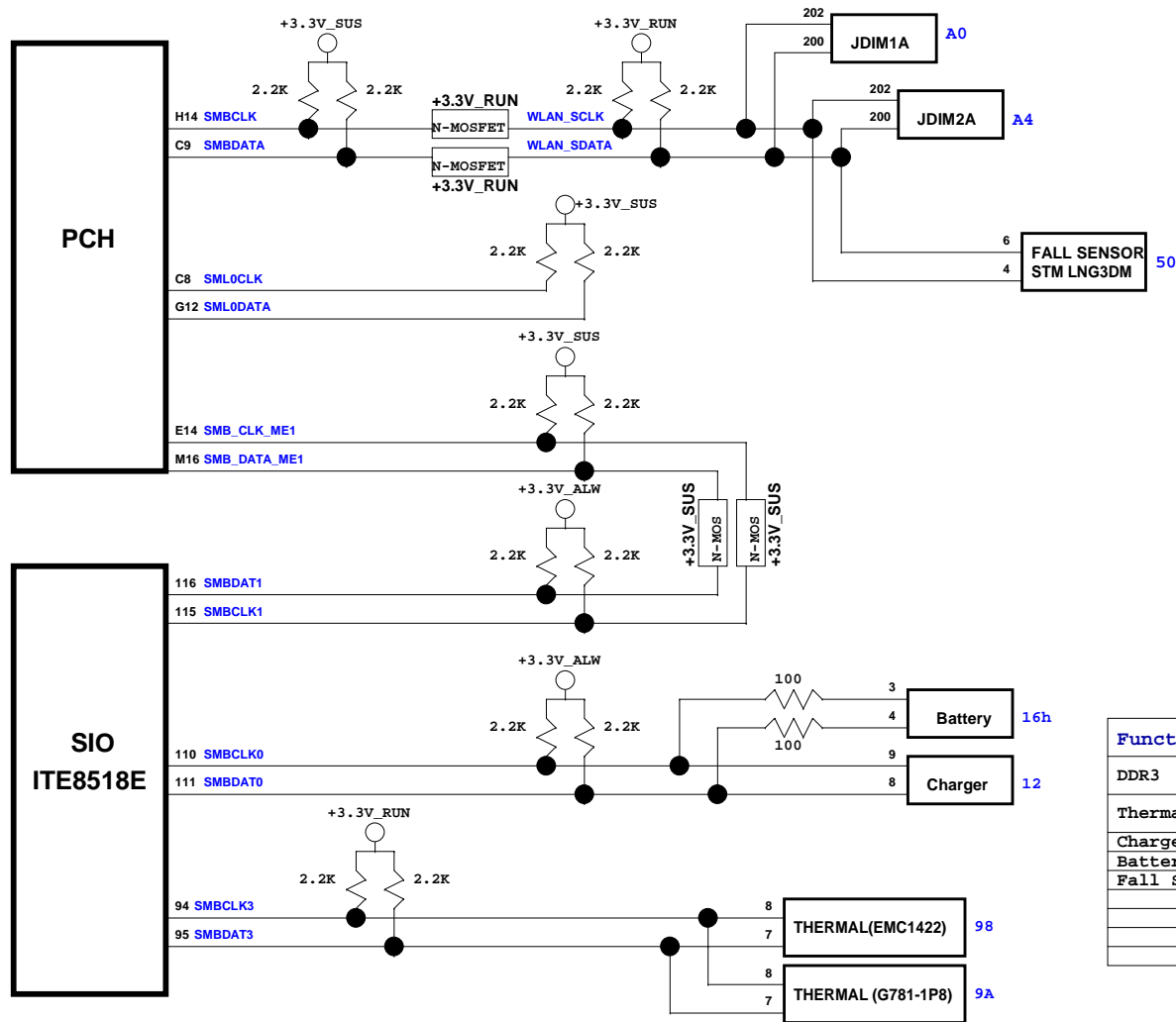


R08/V08 BLOCK DIAGRAM

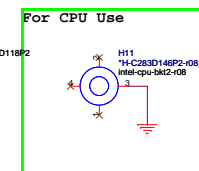
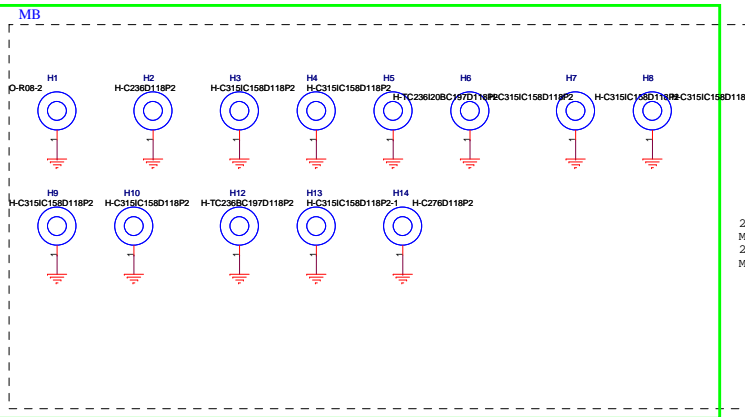
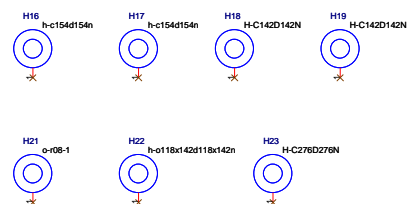


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PROJECT : R08



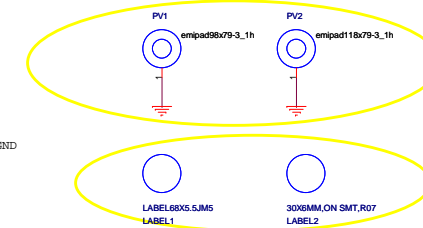
Function	IC	SMBus Address
DDR3	JDIM1A	A0h
	JDIM2A	A4h
Thermal IC	EMC1422	1001100xb (98h)
	G781-1P8	1001101xb (9Ah)
Charge IC	BQ24707ARGRR	0b0001001x (0x12h)
Battery	Battery	16h
Fall Sensor	STM LNG3DM	01010000 (50h)

SCREW PAD



20120206
Modify H11 pin1,2,3,4 no connect to GND
20120209
Modify H11 pin3 connect to GND

20120204
Modify PV1 PV2 subsystem ID to OTH

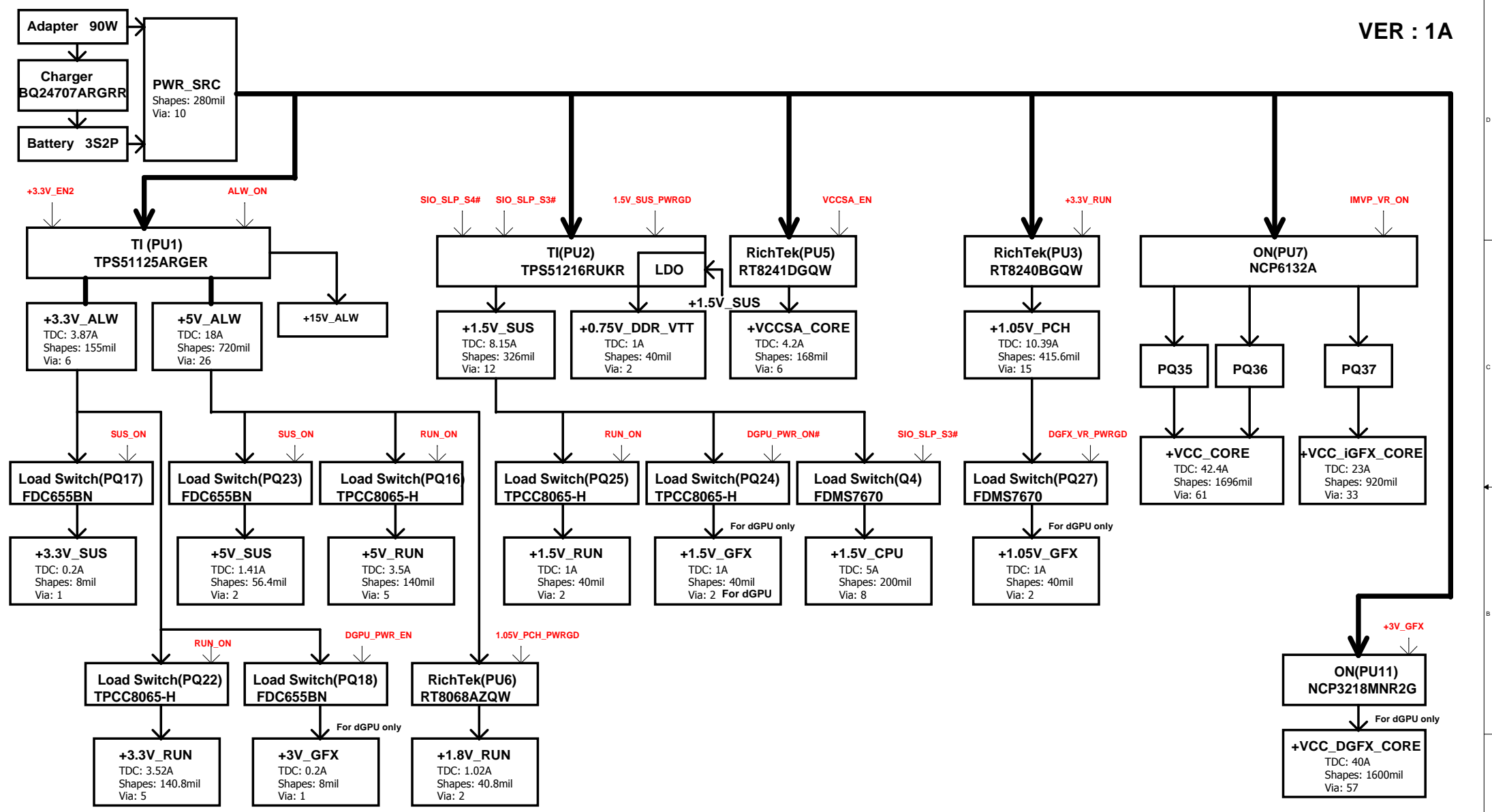


20120204
Add two label PV HCR07003010 and RCM5004013

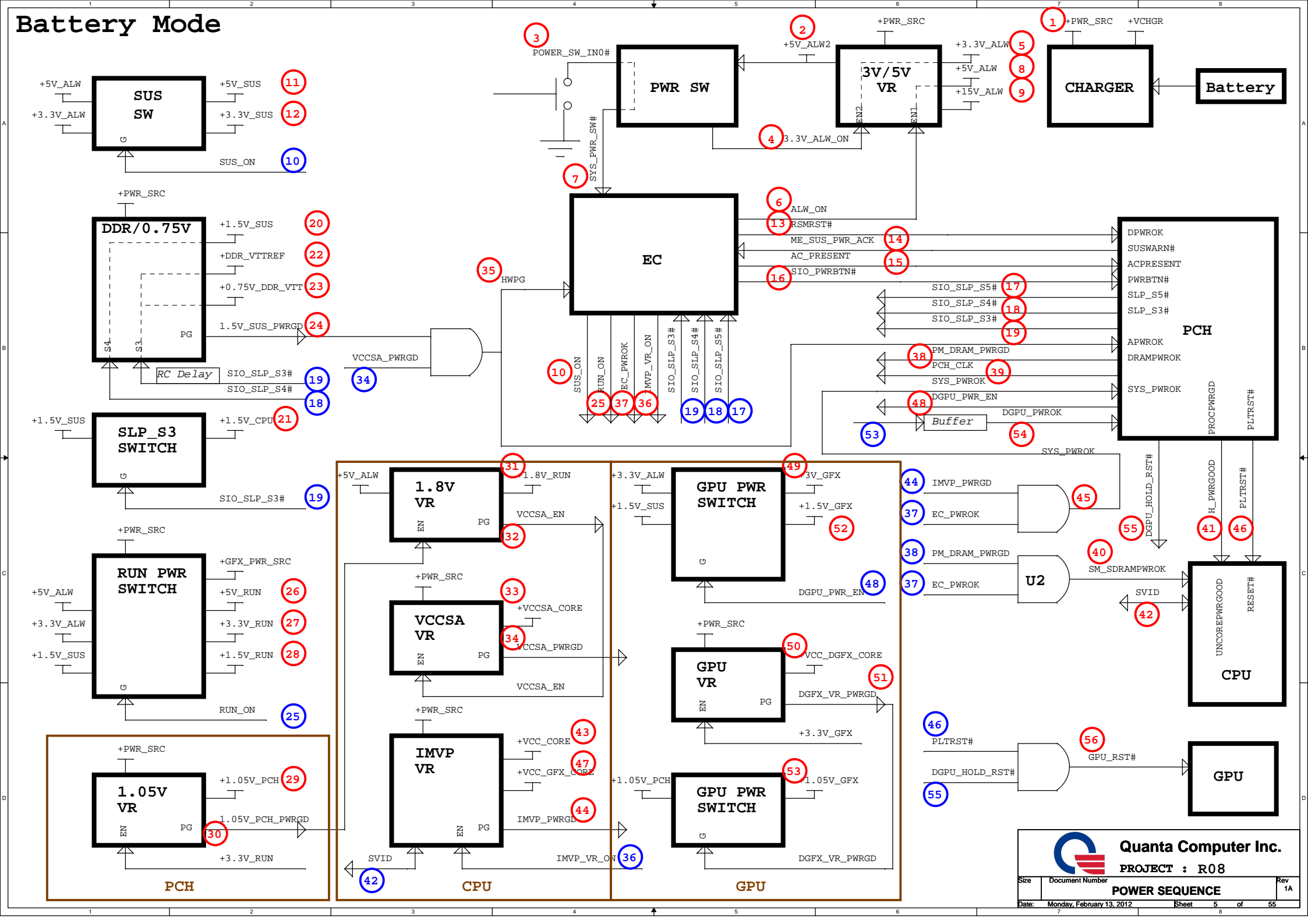
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0/eSATA/ Power share/ debug port)
USB2	External port#3 (USB3.0)
USB3	External port#4 (USB3.0)
USB4	MiniCard 1 (WLAN/BT)
USB5	MiniCard 2 (WWAN/WiMAX)
USB6	X(FOR HM77)
USB7	X(FOR HM77)
USB8	Fingerprint
USB9	Touch panel (NC, for debug)
USB10	Card Reader
USB11	Express Card (NC)
USB12	Camera
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	ODD
SATA4	eSATA (NC)
SATA5	NC

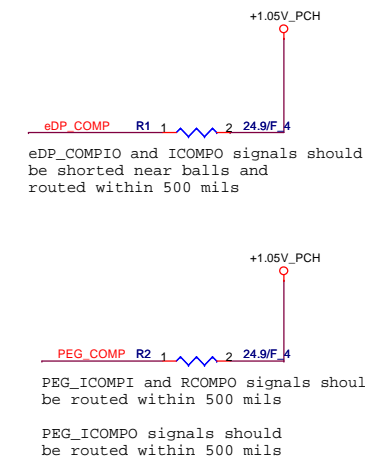
PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	WWAN (NC)
PCIE 3	Card reader (NC)
PCIE 4	NC
PCIE 5	LAN
PCIE 6	Express card (NC)
PCIE 7	NC
PCIE 8	NC



Battery Mode



DP & PEG Compensation



eDP Hot-plug (Disable)

CAD Note: Place PU resistor within 2 inches of CPU

This signal can be left as no connect if entire eDP interface is disabled.

```

3 20120203
3 Change C1~C32 to 0.1U/16V 4 (CH4103K1B08)

```

VGA(U3)	AC coupling Cap	PN	TX location	RX location(page1)
N13P-GL	0.1uF	CH4103K1B08	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185
N13P-GS	0.22uF	CH4223K1B00	C1~C32	C144 C145 C147 C149 C150 C152 C154 C156 C157 C158 C159 C160 C161 C162 C163 C164 C165 C166 C167 C168 C169 C171 C173 C175 C176 C177 C178 C179 C180 C182 C184 C185



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Size	Document Number	Rev
	Ivy Bridge 1/5	1A
Date:	Monday, February 13, 2012	Sheet 6 of 55

Ivy Bridge Processor (CLK,MISC,JTAG)

SNB_IVB# N.A at SNB EDS #27637 0.7v1

23 H_SNB_IVB# ← H_SNB_IVB# C26
38 H_CPUDET# ← H_CPUDET# AN34

TP1 CATERR# ← CATERR# AL33

38 PECI_EC ← PECI_EC R6 1 2 43 4 PECI_EC_R AN33

38,52,54 IMVP7_PROCHOT# ← IMVP7_PROCHOT# R7 1 2 56 4 H_PROCHOT# AL32

Over 130 degree C will drive low
25 PM_THRMTRIP# ← PM_THRMTRIP# AN32

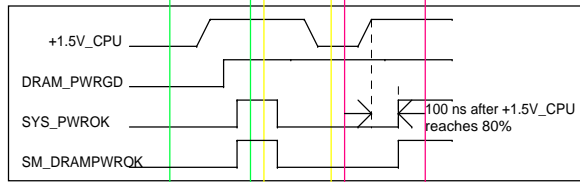
20 H_PM_SYNC ← H_PM_SYNC AM34

25 H_PWRGOOD ← H_PWRGOOD AP33
10K 4 2 1 R17
SM_DRAMPWROK V8

13,23,35,38 PLTRST# ← PLTRST# R19 2 1 1.5K 4 CPU_PLTRST# R AR33
R20 750F 4

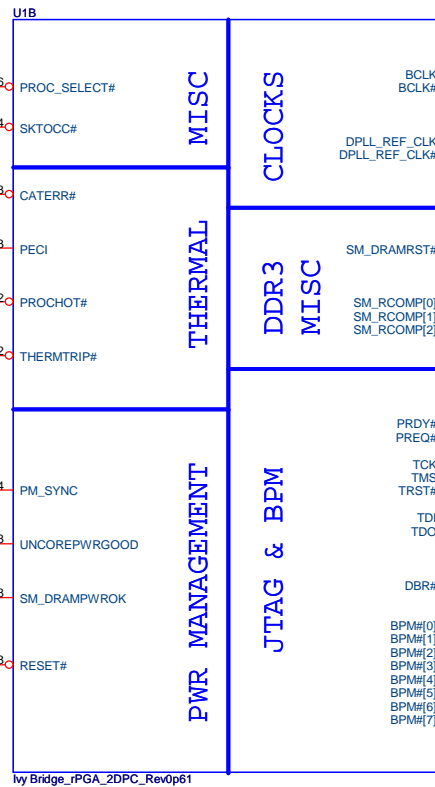
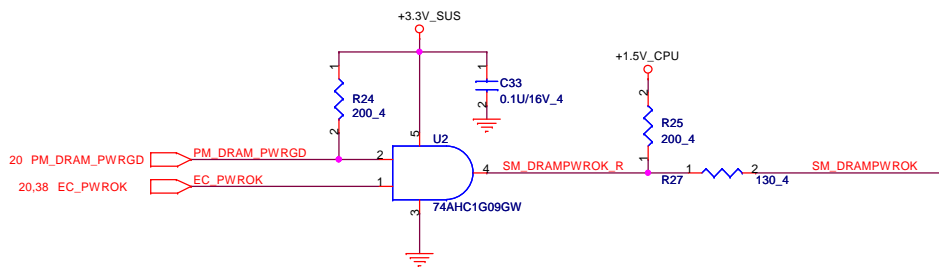
Intel spec VinH min =VCCIO X 0.7

C854 2 1 *100P/50V 4 NC H_PROCHOT#
C860 2 1 *100P/50V 4 NC CPU_PLTRST# R



Follow #DG1.5 471984 P119

Follow #DG1.5 471984 P128
DDR Power Gating Topology



CLOCKS

DDR3 MISC

JTAG & BPM

BCLK CPU BCLKP CLK_CPU_BCLKP 24
BCLK CPU BCLKN CLK_CPU_BCLKN 24

A16 CLK_DP_P_R R4 1 2 1K 4
A15 CLK_DP_N_R R5 1 2 1K 4 +1.05V_PCH

For eDP

SM_DRAMRST# R8 CPU_DRAMRST#

Ak1 SM_RCOMP_0 R8 1 2 140F 4
A5 SM_RCOMP_1 R9 1 2 25.5F 4
A4 SM_RCOMP_2 R10 1 2 200F 4

SM_RCOMP_0, SM_RCOMP_1 20mil / SM_RCOMP_2 15mil.

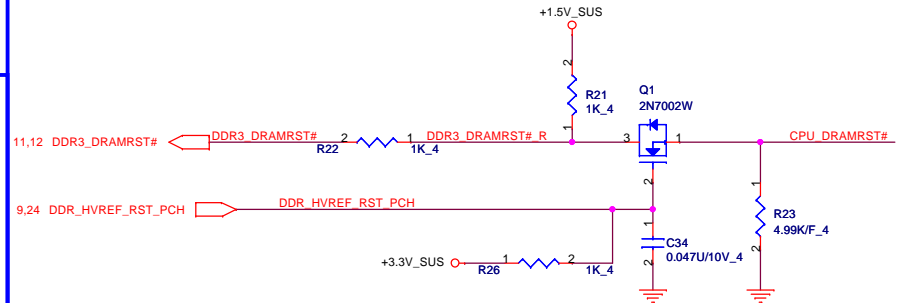
PRDY# AP29
PREQ# AP27
TCK AR26 XDP_TCLK TP28
TMS AR27 XDP_TMS TP37
TRST# AP30 XDP_TRST# TP38
TDI AR28 XDP_TDI TP41
TDO AP26 XDP_TDO TP42

DBR# AL35 XDP_DBRST# R18 1 2 1K 4 +3.3V_RUN

BPM#0 AT28
BPM#1 AR29
BPM#2 AR30
BPM#3 AT30
BPM#4 AP32
BPM#5 AR31
BPM#6 AT31
BPM#7 AR32

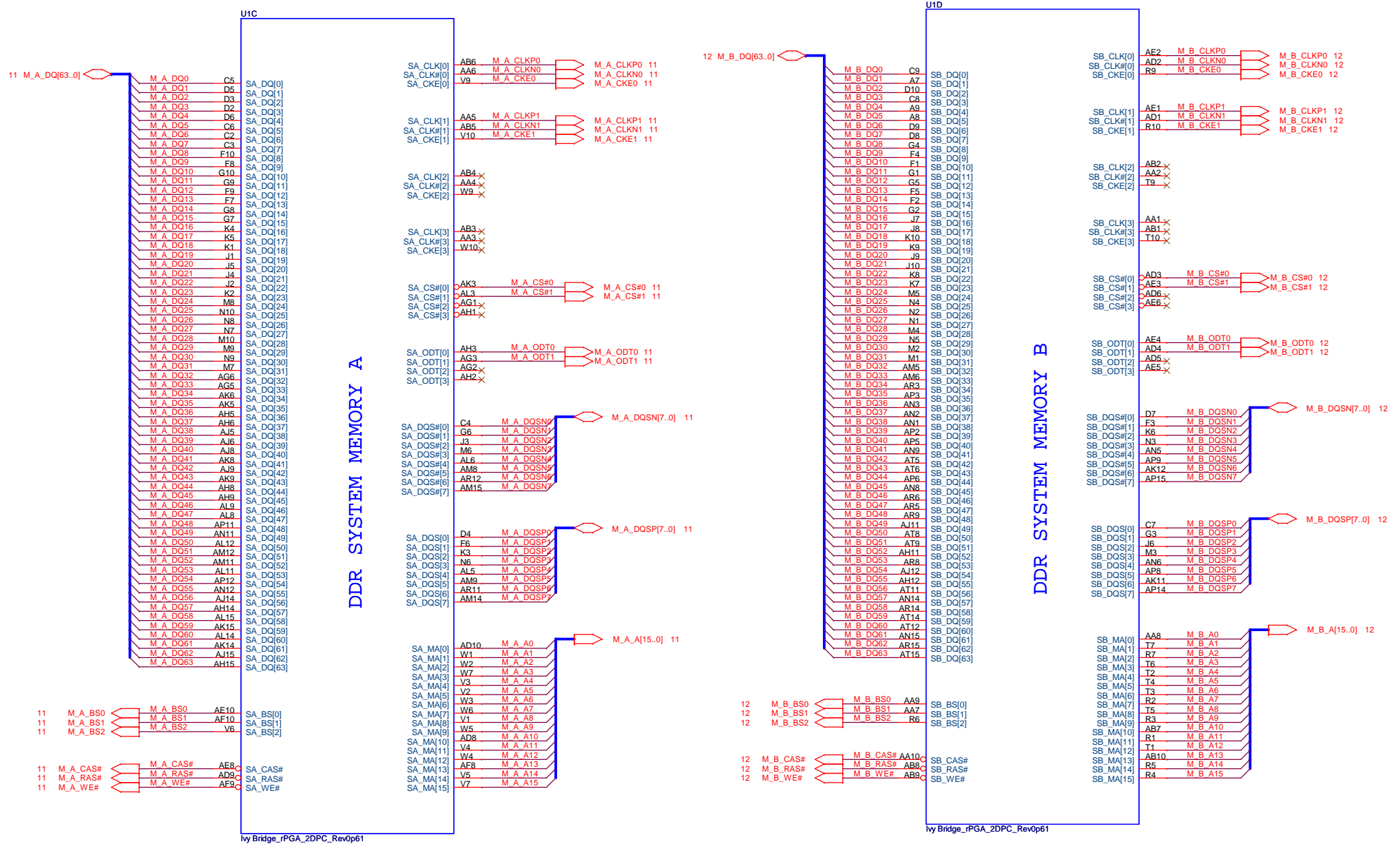
IMVP7_PROCHOT# R14 2 1 62 4 +1.05V_PCH

Follow #DG1.5 471984 P130
DRAMRST# Routing Illustration



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PROJECT : R08

Ivy Bridge Processor (DDR3)



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PROJECT : R08

Ivy Bridge Processor

CPU Core Power
SNB: 53A
IVY: 53A
10uF x 24

+VCC_CORE

POWER

POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

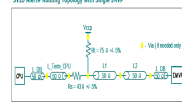
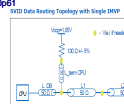
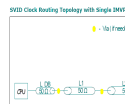
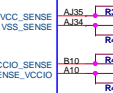
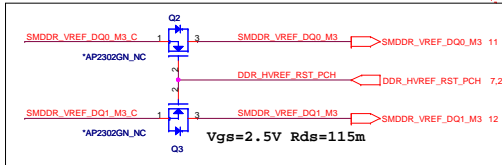
1.05V_PCH

SNB: 8.5A
IVY: 8.5A
10F x12

+1.05V_PCH

Power Rail Sense Line	R1, R2	Trace Impedance	Trace Length Match
VCC_SENSE / VSS_SENSE	100Ω	27-33Ω	<25 mils
VCCAXG_SENSE / VSSAXG_SENSE	100Ω		
VCCIO_SENSE / VSS_SENSE_VCCIO	10Ω	55Ω	
VCCSA	100Ω		

M3 VREF



Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

VR_SVID_CLK → VR_SVID_CLK 52

Place PU resistor close to CPU

SVID DATA

+1.05V_PCH

R45 130.4

VR_SVID_DATA → VR_SVID_DATA 52

Place PU resistor close to CPU

SVID ALERT

+1.05V_PCH

R46 75F.4

H_CPU_SVIDALRT# → VR_SVID_ALERT# 52

Ivy Bridge Processor (GRAPHIC POWER)

POWER

GRAPHICS

1.8V RAIL

SENSE LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

+VCC GFX_CORE

CPU VGT
SNB: 21.5A
IVY: 33A
10uF x 12

UIG

AT24 VAXG1

AT23 VAXG2

AT22 VAXG3

AT21 VAXG4

AT20 VAXG5

AT19 VAXG6

AT18 VAXG7

AT17 VAXG8

AT16 VAXG9

AT15 VAXG10

AT14 VAXG11

AT13 VAXG12

AT12 VAXG13

AT11 VAXG14

AT10 VAXG15

AT09 VAXG16

AT08 VAXG17

AT07 VAXG18

AT06 VAXG19

AT05 VAXG20

AT04 VAXG21

AT03 VAXG22

AT02 VAXG23

AT01 VAXG24

AT00 VAXG25

AT00 VAXG26

AT00 VAXG27

AT00 VAXG28

AT00 VAXG29

AT00 VAXG30

AT00 VAXG31

AT00 VAXG32

AT00 VAXG33

AT00 VAXG34

AT00 VAXG35

AT00 VAXG36

AT00 VAXG37

AT00 VAXG38

AT00 VAXG39

AT00 VAXG40

AT00 VAXG41

AT00 VAXG42

AT00 VAXG43

AT00 VAXG44

AT00 VAXG45

AT00 VAXG46

AT00 VAXG47

AT00 VAXG48

AT00 VAXG49

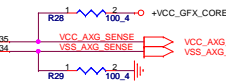
AT00 VAXG50

AT00 VAXG51

AT00 VAXG52

AT00 VAXG53

AT00 VAXG54



+VDDR_REF_CPU → +VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SMDR_VREF_DQ0_M3_C

SMDR_VREF_DQ1_M3_C

R30 1K.4_NC

R31 1K.4_NC

SNB: 5A

IVY: 5A

10uF x 6

+1.5V_CPU

VDDQ1 VDDQ2

VDDQ3 VDDQ4

VDDQ5 VDDQ6

VDDQ7 VDDQ8

VDDQ9 VDDQ10

VDDQ11 VDDQ12

VDDQ13 VDDQ14

VDDQ15 VDDQ16

VDDQ17 VDDQ18

VDDQ19 VDDQ20

VDDQ21 VDDQ22

VDDQ23 VDDQ24

VDDQ25 VDDQ26

VDDQ27 VDDQ28

VDDQ29 VDDQ30

VDDQ31 VDDQ32

VDDQ33 VDDQ34

VDDQ35 VDDQ36

VDDQ37 VDDQ38

VDDQ39 VDDQ40

VDDQ41 VDDQ42

VDDQ43 VDDQ44

VDDQ45 VDDQ46

VDDQ47 VDDQ48

VDDQ49 VDDQ50

VDDQ51 VDDQ52

VDDQ53 VDDQ54

VDDQ55 VDDQ56

VDDQ57 VDDQ58

VDDQ59 VDDQ60

VDDQ61 VDDQ62

VDDQ63 VDDQ64

VDDQ65 VDDQ66

VDDQ67 VDDQ68

VDDQ69 VDDQ70

VDDQ71 VDDQ72

VDDQ73 VDDQ74

VDDQ75 VDDQ76

VDDQ77 VDDQ78

VDDQ79 VDDQ80

VDDQ81 VDDQ82

VDDQ83 VDDQ84

VDDQ85 VDDQ86

VDDQ87 VDDQ88

VDDQ89 VDDQ90

VDDQ91 VDDQ92

VDDQ93 VDDQ94

VDDQ95 VDDQ96

VDDQ97 VDDQ98

VDDQ99 VDDQ100

VDDQ101 VDDQ102

VDDQ103 VDDQ104

VDDQ105 VDDQ106

VDDQ107 VDDQ108

VDDQ109 VDDQ110

VDDQ111 VDDQ112

VDDQ113 VDDQ114

VDDQ115 VDDQ116

VDDQ117 VDDQ118

VDDQ119 VDDQ120

VDDQ121 VDDQ122

VDDQ123 VDDQ124

VDDQ125 VDDQ126

VDDQ127 VDDQ128

VDDQ129 VDDQ130

VDDQ131 VDDQ132

VDDQ133 VDDQ134

VDDQ135 VDDQ136

VDDQ137 VDDQ138

VDDQ139 VDDQ140

VDDQ141 VDDQ142

VDDQ143 VDDQ144

VDDQ145 VDDQ146

VDDQ147 VDDQ148

VDDQ149 VDDQ150

VDDQ151 VDDQ152

VDDQ153 VDDQ154

VDDQ155 VDDQ156

VDDQ157 VDDQ158

VDDQ159 VDDQ160

VDDQ161 VDDQ162

VDDQ163 VDDQ164

VDDQ165 VDDQ166

VDDQ167 VDDQ168

VDDQ169 VDDQ170

VDDQ171 VDDQ172

VDDQ173 VDDQ174

VDDQ175 VDDQ176

VDDQ177 VDDQ178

VDDQ179 VDDQ180

VDDQ181 VDDQ182

VDDQ183 VDDQ184

VDDQ185 VDDQ186

VDDQ187 VDDQ188

VDDQ189 VDDQ190

VDDQ191 VDDQ192

VDDQ193 VDDQ194

VDDQ195 VDDQ196

VDDQ197 VDDQ198

VDDQ199 VDDQ200

VDDQ201 VDDQ202

VDDQ203 VDDQ204

VDDQ205 VDDQ206

VDDQ207 VDDQ208

VDDQ209 VDDQ210

VDDQ211 VDDQ212

VDDQ213 VDDQ214

VDDQ215 VDDQ216

VDDQ217 VDDQ218

VDDQ219 VDDQ220

VDDQ221 VDDQ222

VDDQ223 VDDQ224

VDDQ225 VDDQ226

VDDQ227 VDDQ228

VDDQ229 VDDQ230

VDDQ231 VDDQ232

VDDQ233 VDDQ234

VDDQ235 VDDQ236

VDDQ237 VDDQ238

VDDQ239 VDDQ240

VDDQ241 VDDQ242

VDDQ243 VDDQ244

VDDQ245 VDDQ246

VDDQ247 VDDQ248

VDDQ249 VDDQ250

VDDQ251 VDDQ252

VDDQ253 VDDQ254

VDDQ255 VDDQ256

VDDQ257 VDDQ258

VDDQ259 VDDQ260

VDDQ261 VDDQ262

VDDQ263 VDDQ264

VDDQ265 VDDQ266

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VDDQ271 VDDQ272

VDDQ273 VDDQ274

VDDQ275 VDDQ276

VDDQ277 VDDQ278

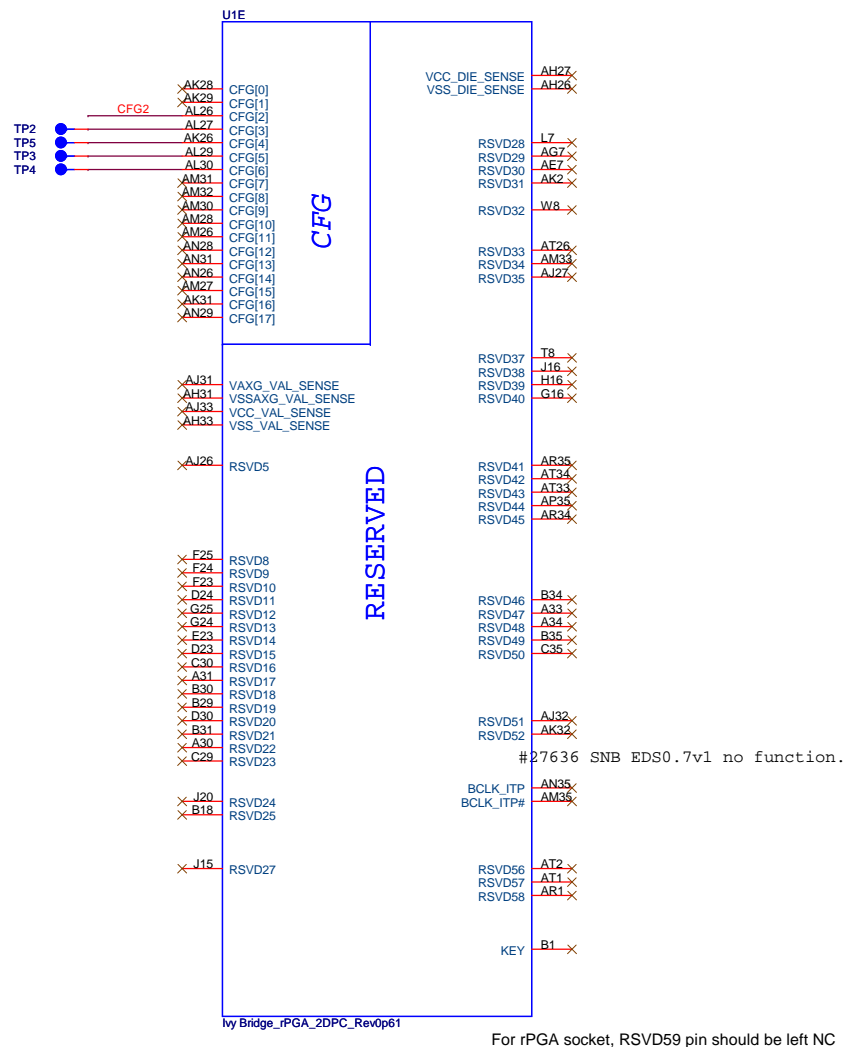
VDDQ279 VDDQ280

VDDQ281 VDDQ282

VDDQ283 VDDQ284

VDDQ285 VDDQ286

Ivy Bridge Processor (RESERVED, CFG)



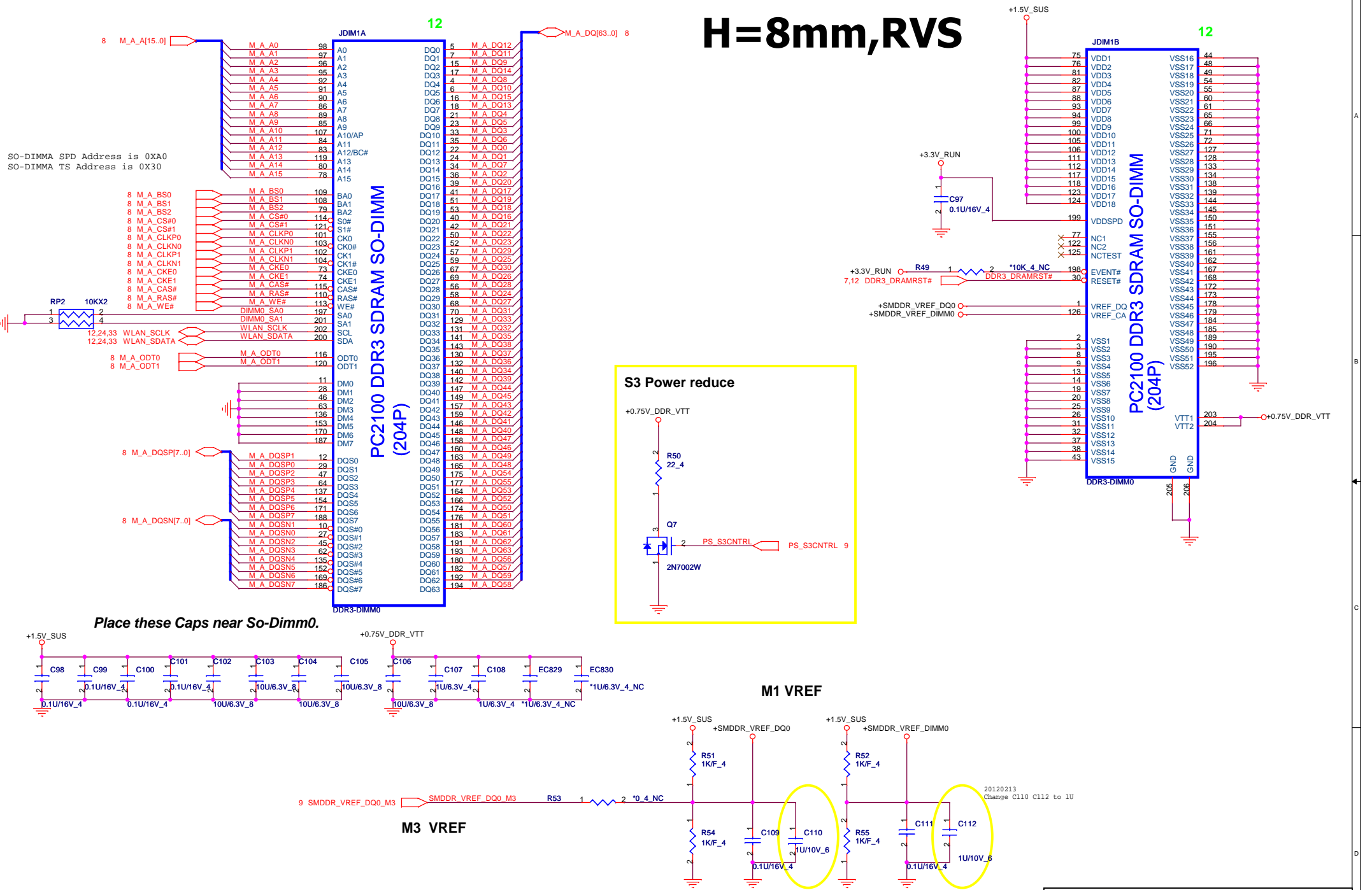
```
11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
```

The CFG signals have a default value of '1' if not terminated on the board.

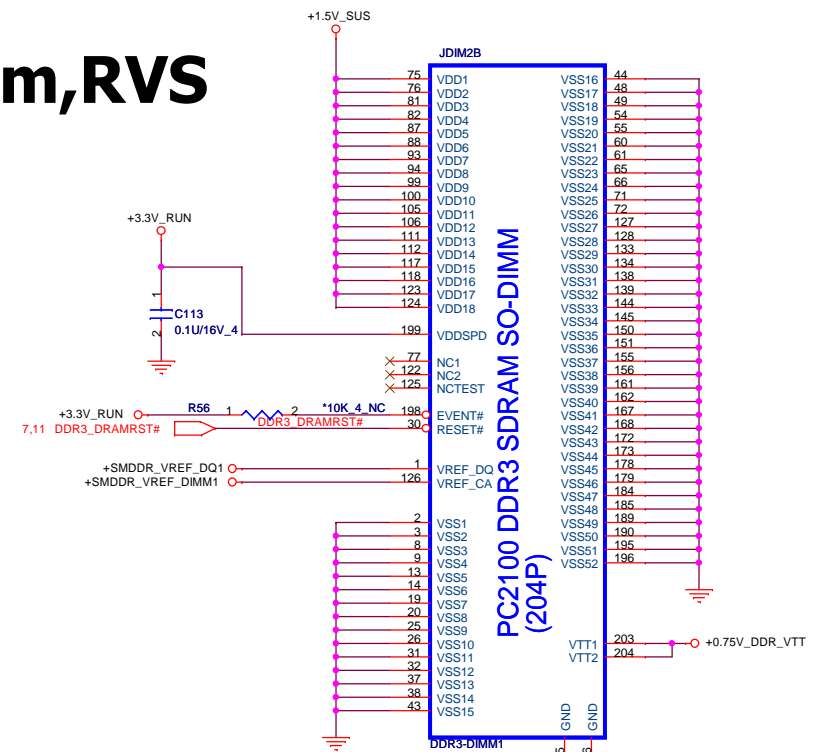
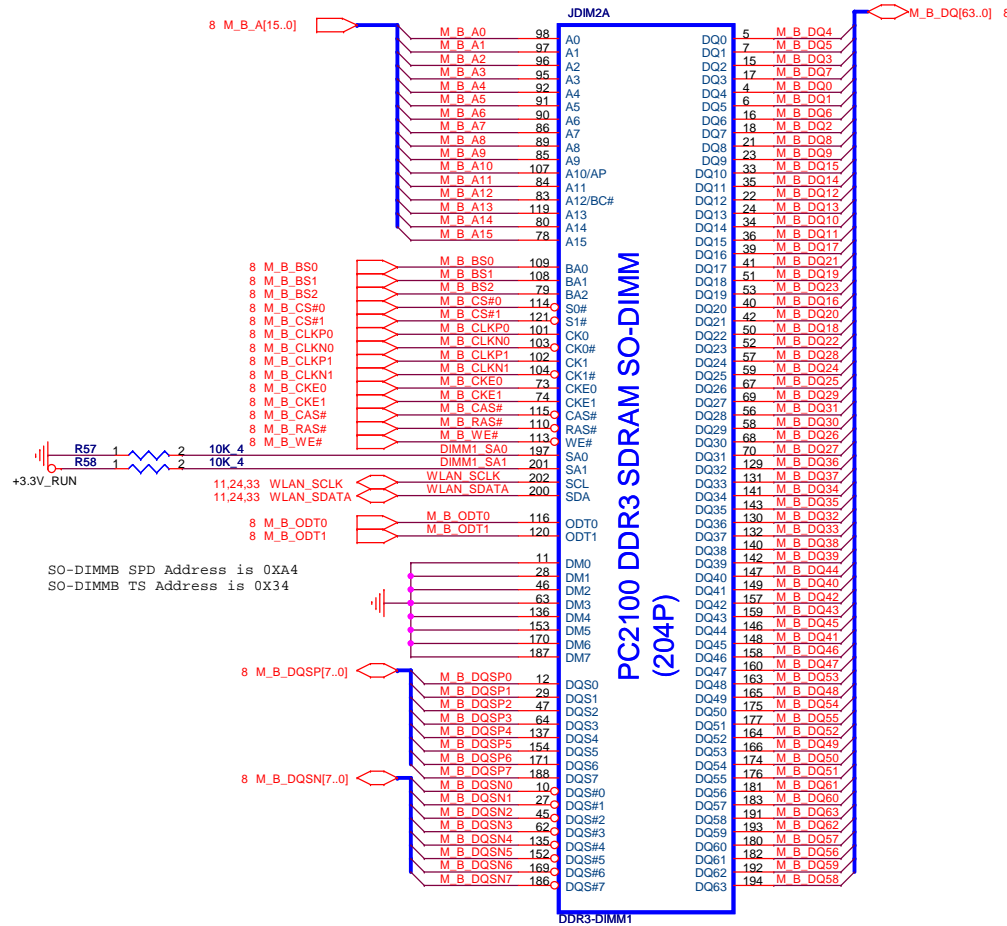


Size	Document Number	Rev
	Ivy Bridge 5/5	1A
Date:	Monday, February 13, 2012	Sheet 10 of 55

H=8mm,RVS



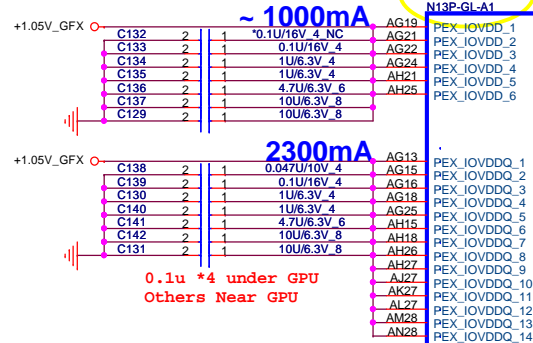
H=4mm,RVS



20120203
Change U3 to AJ0N13P0T02(N13P-GL)
20120204
Change U3 to AJ0N13P0T49(WINCON)

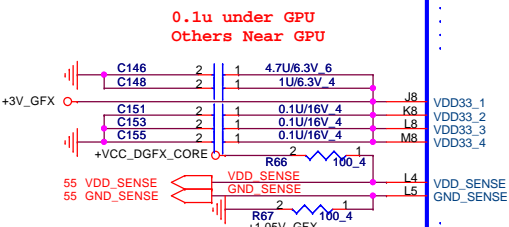
PEX_IOVDD+PEX_IOVDDQ >3.3A

U3A
N13P-GLA1

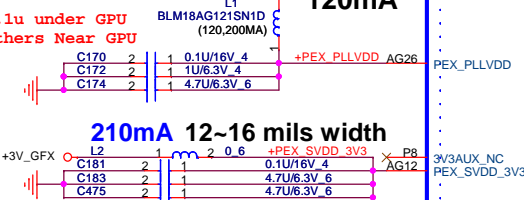


GB4-128

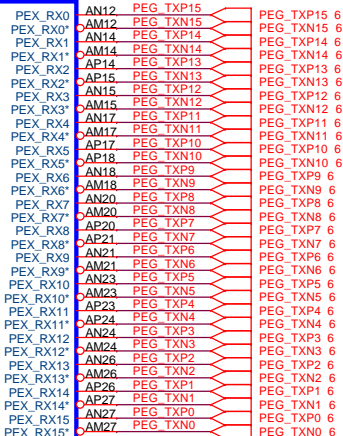
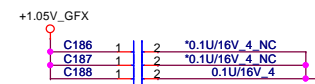
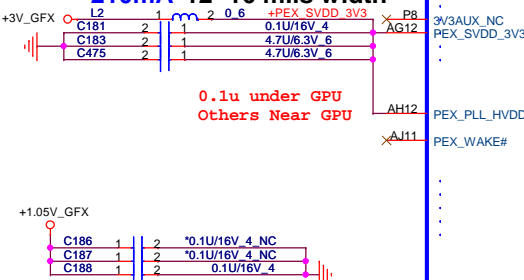
PCI EXPRESS



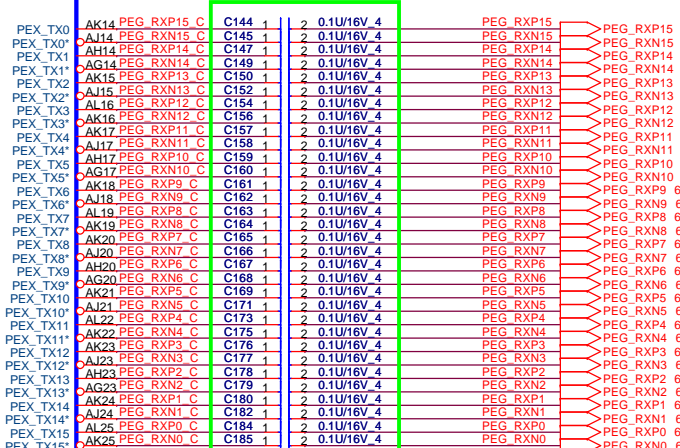
12~16 mils width
120mA



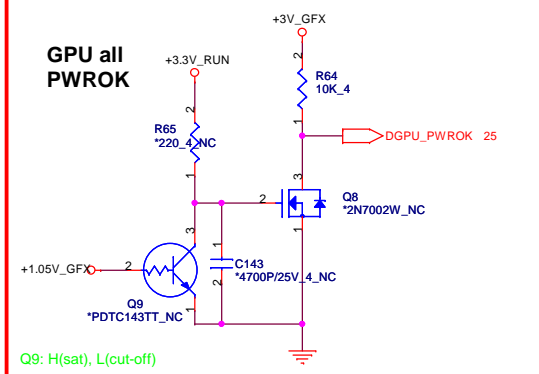
210mA 12~16 mils width



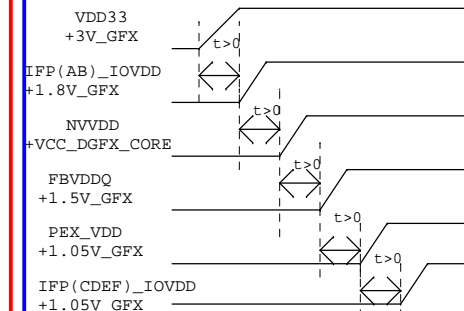
0.22uF AC coupling Caps for PCIE GEN3
0.1uF AC coupling Caps for PCIE GEN1/2



GPU all
PWROK

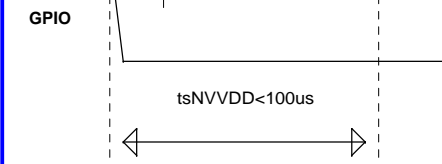
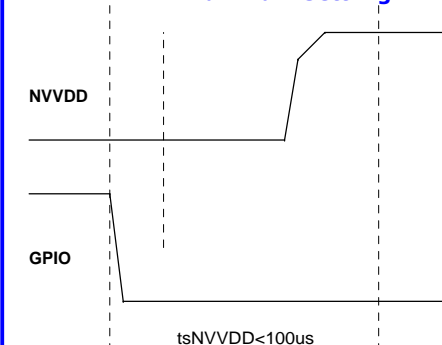


Power up sequence

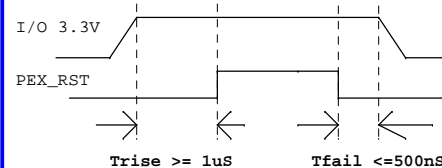


NB9M: VGACORE +0.90V (Normal) , +1.09V

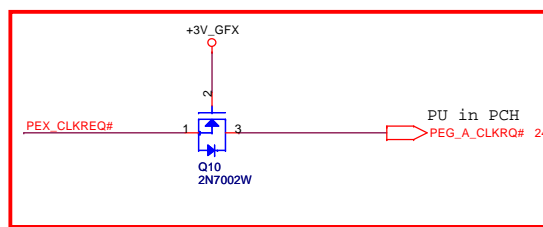
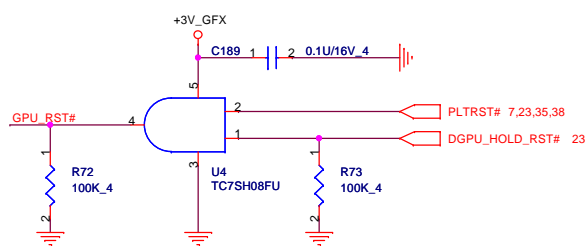
NVVDD Maximum Settling Time



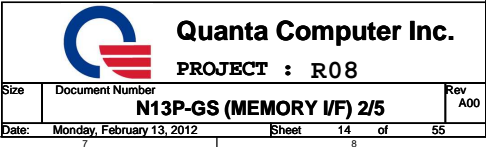
PEX_RST timing



20120203
Change C144 C145 C147 C149 C150
C152 C154 C156 C157 C158
C159 C160 C161 C162 C163
C164 C165 C166 C167 C168
C169 C171 C173 C175 C176
C177 C178 C179 C180 C182
C184 C185 to 0.1U/16V_4(CH4103K1B08)



Quanta Computer Inc.
PROJECT : R08

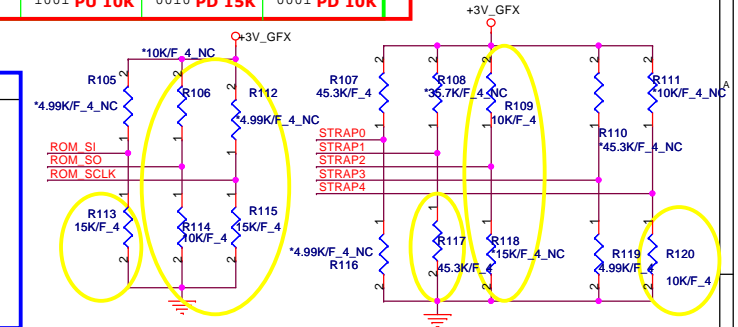


N13P-GL (AJ0N13P0T02)
N13P-GS for Turbo (AJ001070T00)

Strap Bit	Description
USER[3:0]	1111 EDID is used
3GIO_PADCFG [3:0]	0110 Notebook Default
PCI_DEVID[5:0]	D2 PCI Device ID
SORx_EXPOSED [3:0]	0000 Audio capability on each display port Not in use
DP_PLL_VDD33V	1 Default
PCIE_MAX_SPEED GEN3	1 PCIE Gen2/3 capable
PCIE_SPEED_CHANGE GEN3	0 Default
RAMCFG[3:0]	0010 Default Hynix1G
PCIE_PLL_TERMINATION	0 PCIE PLL termination disable (Default)
PEX_PLL_EN_TERM	0 No video BIOS ROM
SUB_VENDOR	01 Frame Buffer size Reserve
FB[1:0]	01
SMB_ALT_ADDR	0 Default (1GPU)
VGA_DEVICE	1 Default (non 3D)

Logical Strap Bit Mapping

	PU-VDD	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

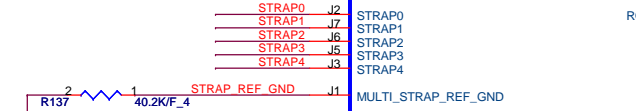
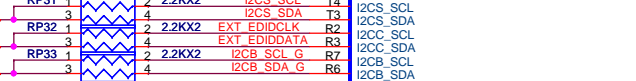
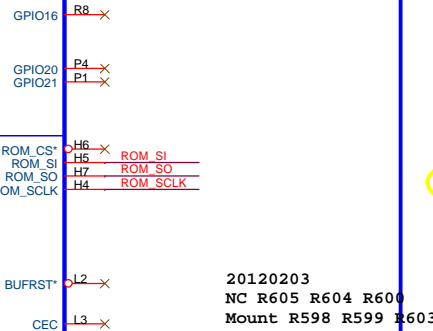
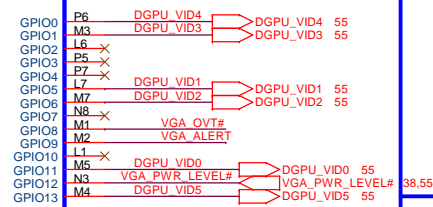
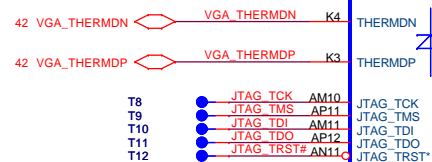


10K/F 4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
4.99K/F 4: CS24992FB26 [RES CHIP 4.99K 1/16W +1% (0402)]
15K/F 4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
20K/F 4: CS32002FB29 [RES CHIP 20K 1/16W +1% (0402)]
24.9K/F 4: CS32492FB16 [RES CHIP 24.9K 1/16W +1% (0402)]
30.1K/F 4: CS33012FB18 [RES CHIP 30.1K 1/16W +1% (0402)]
35.7K/F 4: CS33572FB13 [RES CHIP 35.7K 1/16W +1% (0402)]
45.3K/F 4: CS34532FB18 [RES CHIP 45.3K 1/16W +1% (0402)]

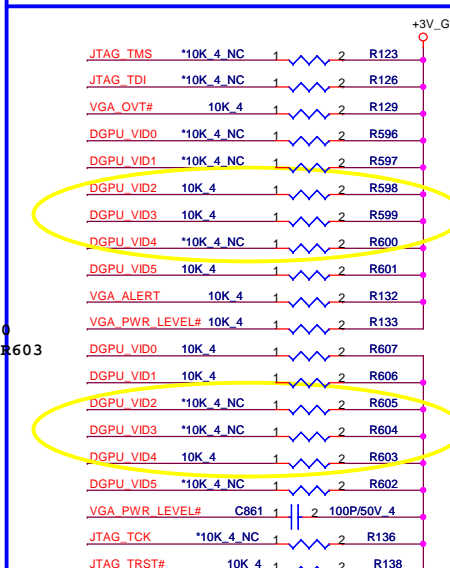
	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	0010
STRAP4	RESERVED	PCI_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	0001
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1001
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0111
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

Default: Hynix VRAM 2G (0110) VRAM Configuration Table


RAMCFG [3:0]	DESCRIPTION	Vendor	Quanta P/N	Vendor P/N	ROM_SI
0000	Reserve	Reserved	Reserve	Reserve	PD 5K
0001	Reserve	Reserved	Reserve	Reserve	PD 10K
0010	DDR3 64Mx16, 900MHz	Hynix	AKD5LZWTW07	H5T1G63DFR-11C	PD 15K
0011	DDR3 64Mx16, 900MHz (G-die)	Samsung	AKD5EGGT509	K4W1G1646G-BC11	PD 20K
0110	DDR3 128Mx16, 900MHz	Hynix	AKD5MGWTW06	H5T1Q638FR-11C	PD 35K
0111	DDR3 128Mx16, 900MHz	Samsung	AKD5MGWT507	K4W2G1646C-HC11	PD 45K



	Output	VID0	VID1	VID2	VID3	VID4	VID5
N13P-GL	0.95V	0	0	1	1	0	1
N13P-GS	0.9V	0	0	0	0	1	1

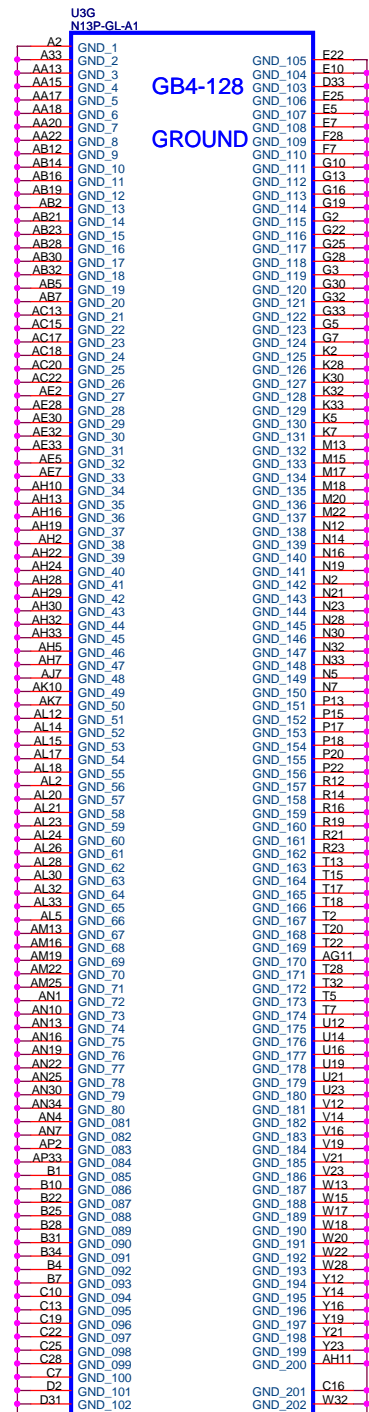
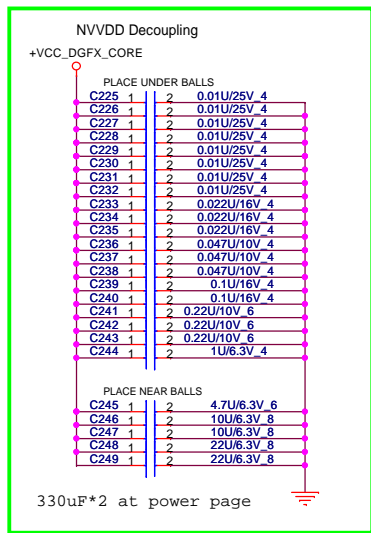
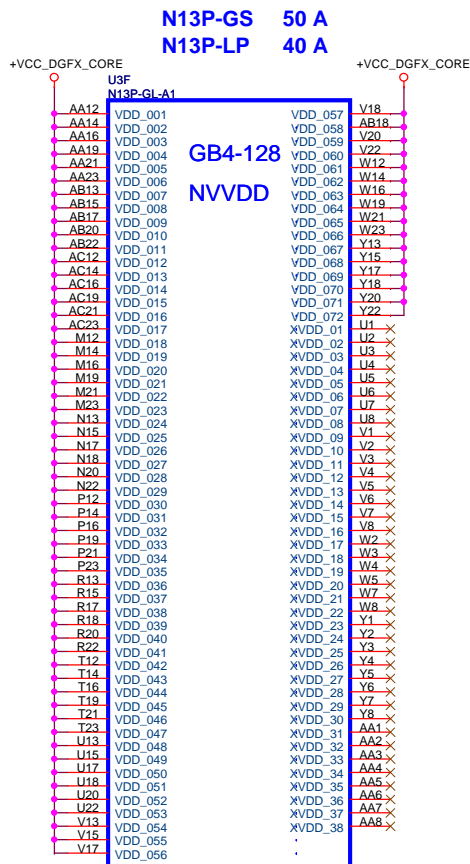


GPIO ASSIGNMENTS			
GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	NVDD_VID4
1	IN	N/A	NVDD_VID3
2	OUT	HIGH	NC
3	OUT	HIGH	NC
4	OUT	HIGH	NC
5	OUT	N/A	NVDD_VID1
6	OUT	N/A	NVDD_VID2
7	OUT	N/A	NC
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	NC
11	OUT	N/A	NVDD_VID0
12	IN	N/A	PWR_LEVEL
13	OUT	N/A	NVDD_VID5

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PROJECT : R08

Size: Document Number: **N13P-GS (GPIO&STRAPS) 4/5** Rev: A00

Date: Monday, February 13, 2012 Sheet: 16 of 55



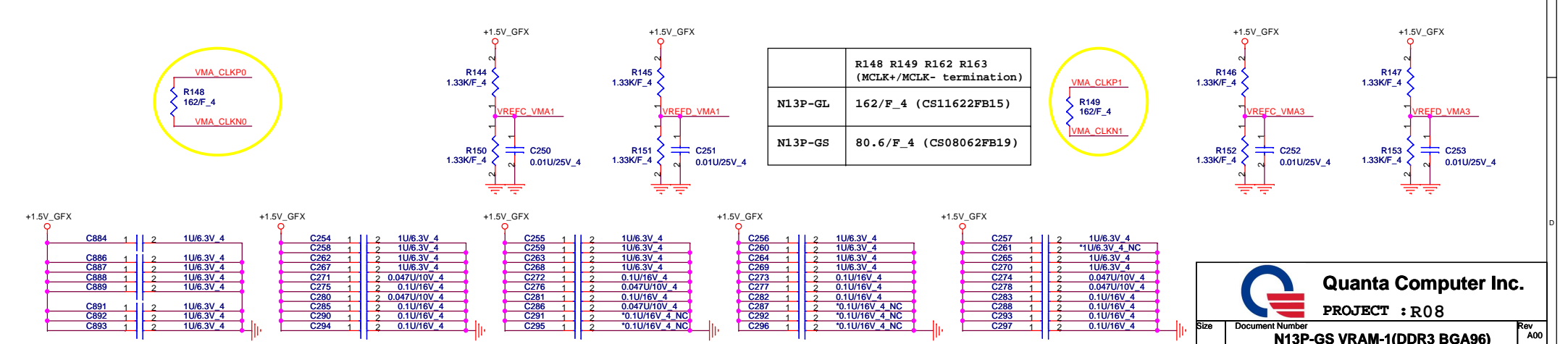
Quanta Computer Inc.

PROJECT : R08

Change U6~U13 to AKD5LZWTW07 (hynix 1G)

```
14 VMA_DQ[63..0]  •
14 VMA_DM[7..0]   •
14 VMA_WDQS[7..0] •
14 VMA_RDQS[7..0] •
```

CHANNEL A: 512MB/1024MB DDR3



	R148 R149 R162 R163 (MCLK+/MCLK- termination)
N13P-GL	162/F_4 (CS11622FB15)
N13P-GS	80.6/F_4 (CS08062FB19)

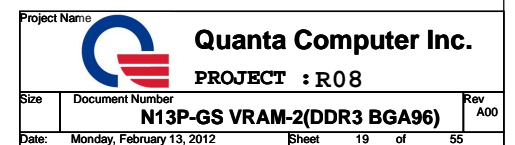
Quanta Computer Inc.

PROJECT : R08

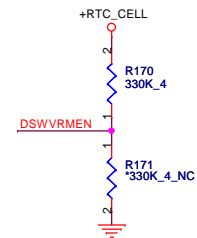
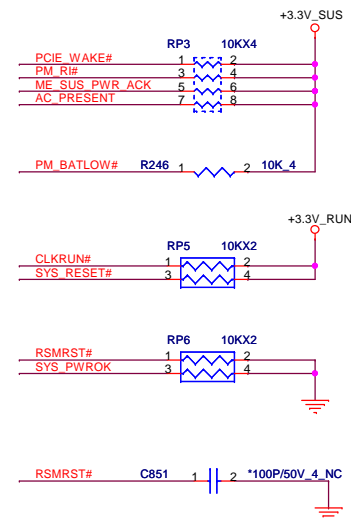
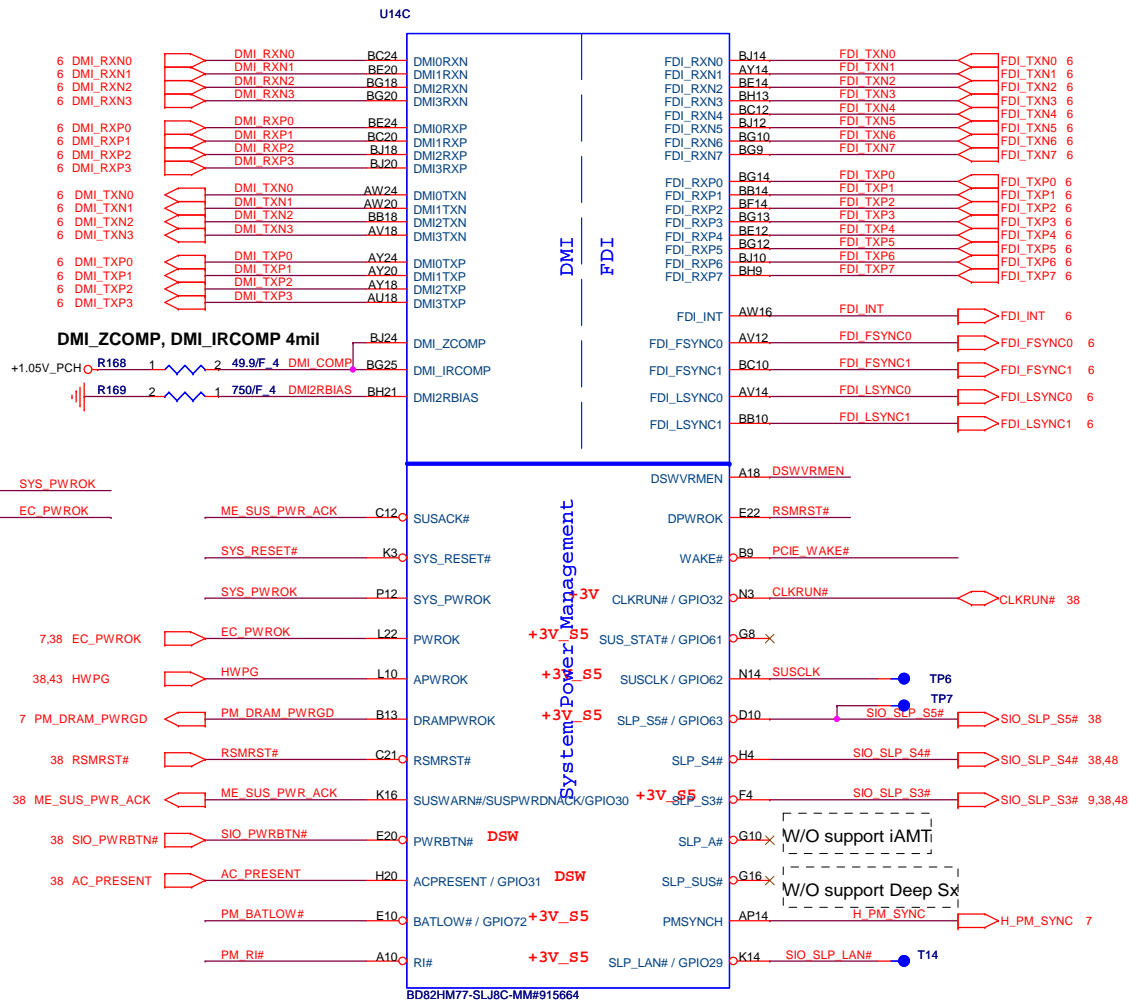
Size	Document Number	Rev
	11429-00-000-1 (PDRS-2010-01)	000

Date: Monday, February 13, 2012 Sheet 18 of 55

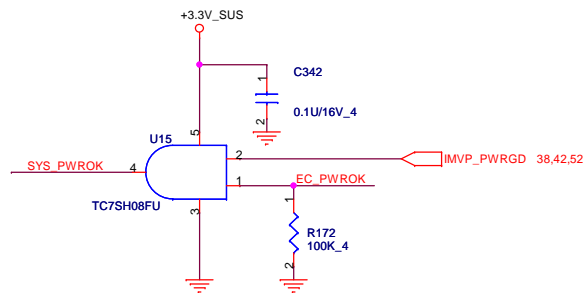
14 VMC_DQ[63..0]
14 VMC_DM[7..0]
14 VMC_WDQS[7..0]
14 VMC_RDQS[7..0]



Cougar Point/Panther Point (DMI,FDI,PM)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

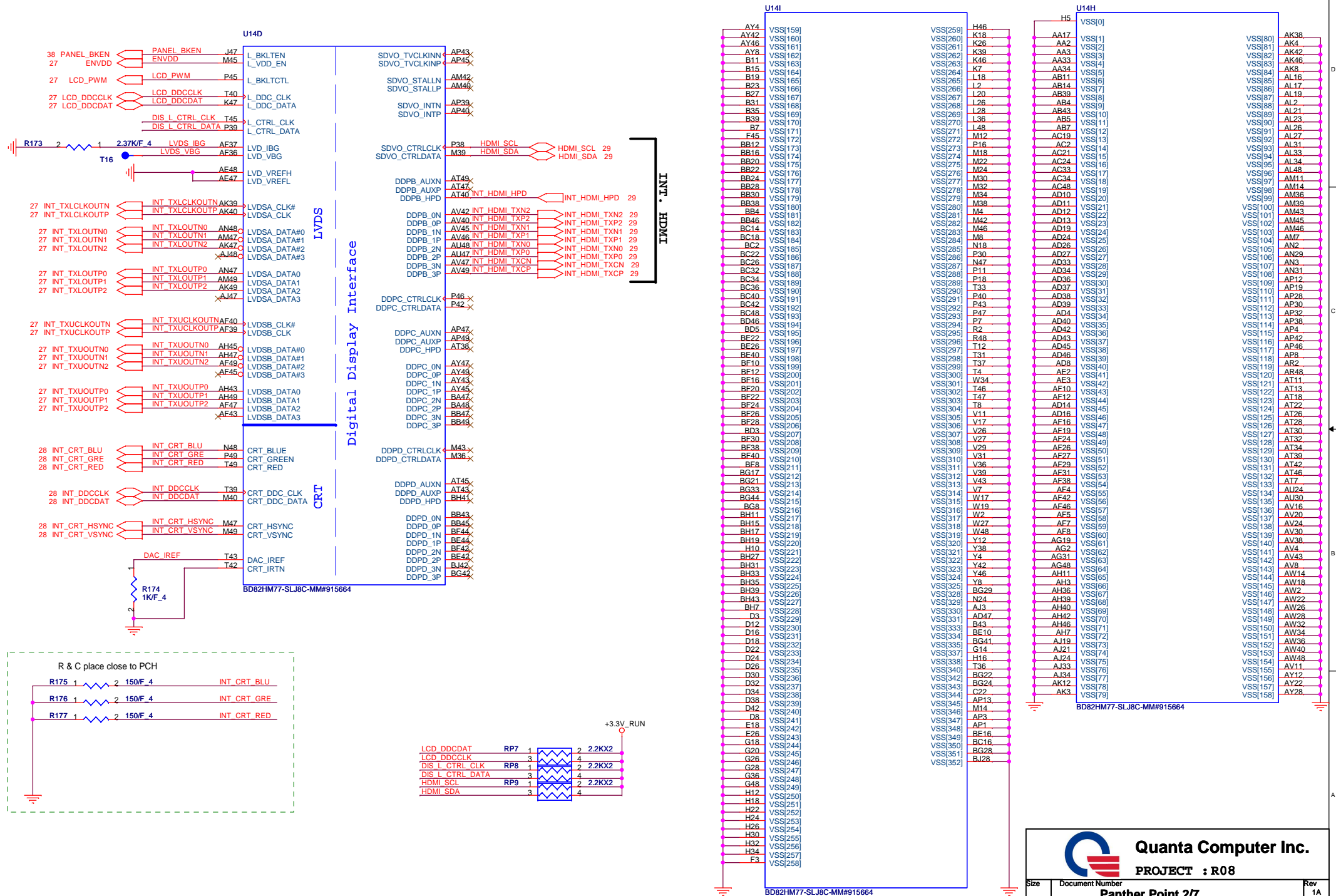
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PROJECT : R08

Panther Point 1/7

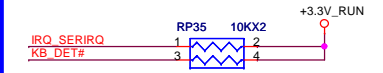
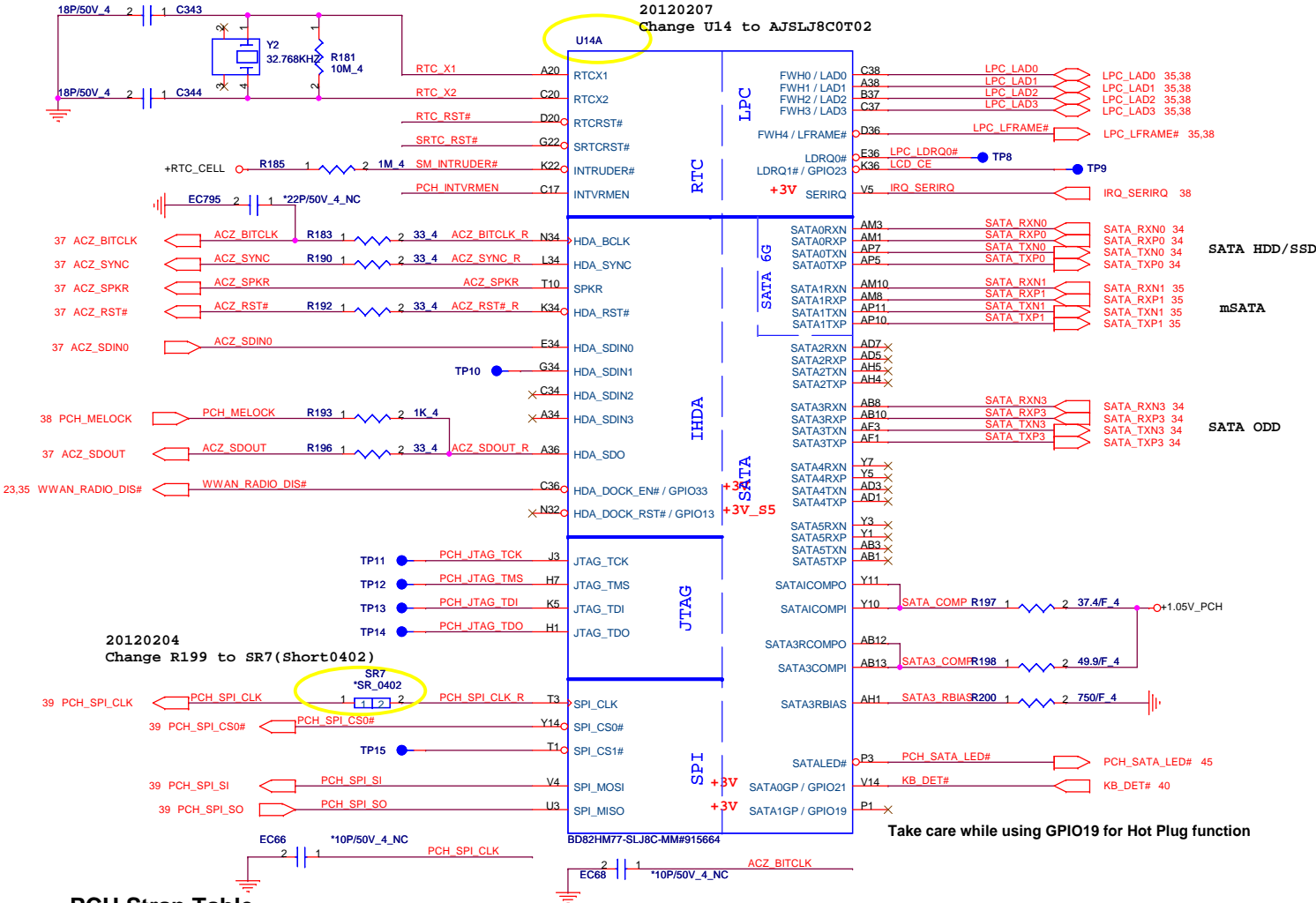
Size	Document Number Panther Point 1/7	Rev 1A
Date:	Monday, February 13, 2012	Sheet 20 of 55

Cougar Point/Panther Point (GND)

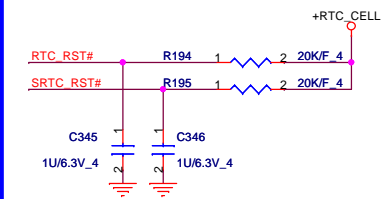


Cougar Point/Panther Point (HDA,JTAG,SATA)

20120204
Change U14 to AJ0QPEG0T07(WINCON)
20120207
Change U14 to AJSLJ8C0T02



MP remove(Intel)(JTAG)

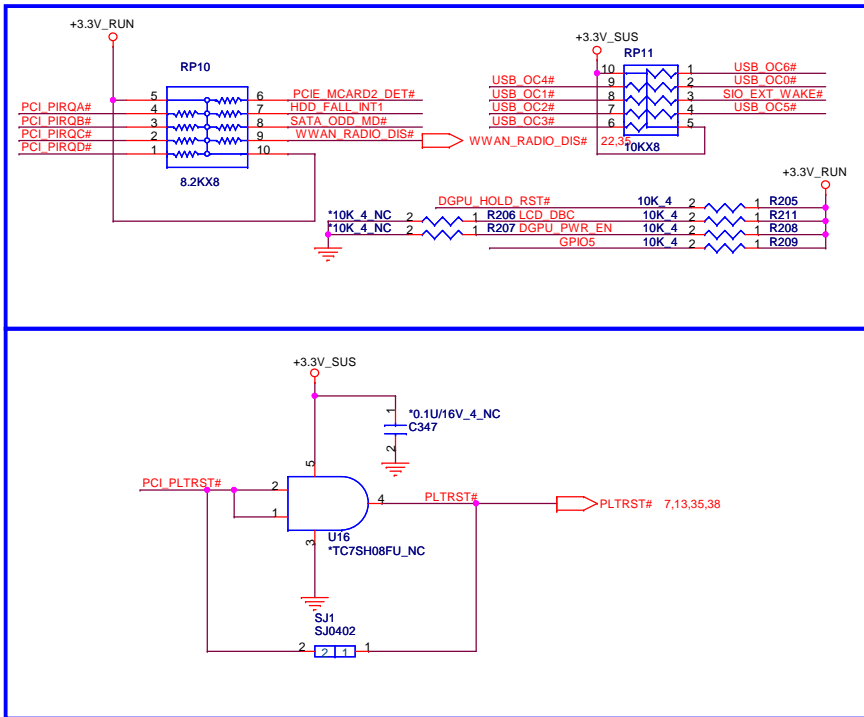


Take care while using GPIO19 for Hot Plug function

PCH Strap Table

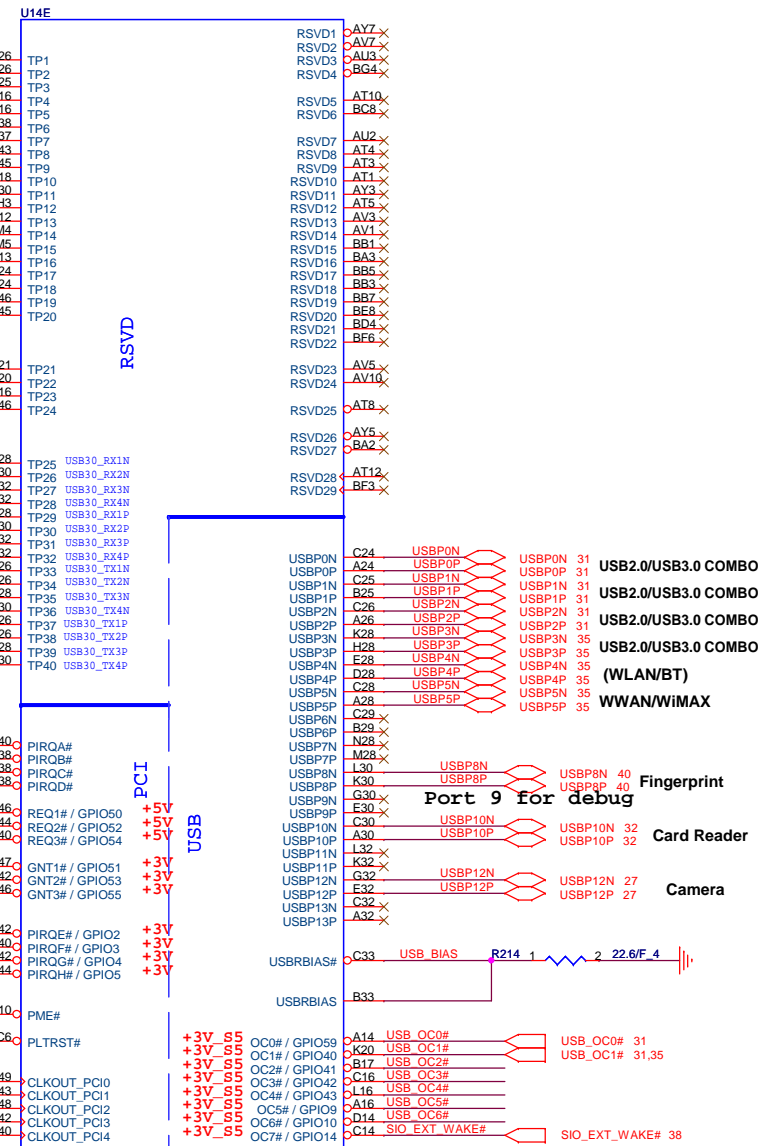
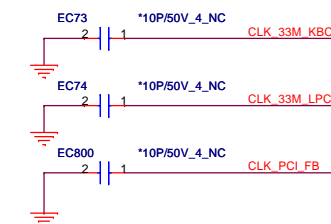
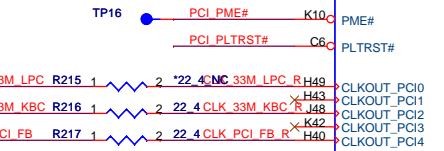
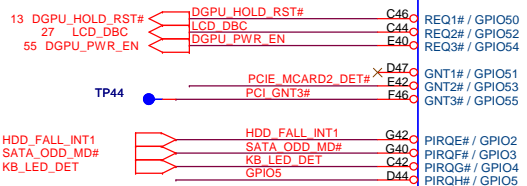
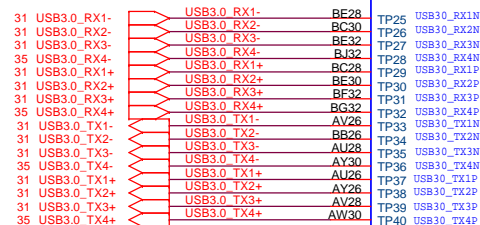
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security	PWROK	0 = Default (weak pull-down 20K) 1 = Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL ○R203 1 2 330K 4 PCH_INTVRMEN
HDA_SYNC	On-Die PLL VR Volatge Select	RSMRST	0 = Support by 1.8V (weak PD) 1 = Support by 1.5V	+3.3V_SUS ○R204 1 2 1K 4 ACZ_SYNC_R

Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Pin Name	Strap description	Sampled	Configuration									
GNT2# / GPIO53	ESl strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><td>Bit 0</td><td>Bit 1</td><td>Boot Location</td></tr><tr><td>1</td><td>1</td><td>SPI *</td></tr><tr><td>0</td><td>0</td><td>LPC</td></tr></table>	Bit 0	Bit 1	Boot Location	1	1	SPI *	0	0	LPC
Bit 0	Bit 1	Boot Location										
1	1	SPI *										
0	0	LPC										
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK										
Default weak pull-up on GNT0/1# [Need external pull-down for LPC BIOS]												
DF_TVS	DMI and FDI Tx/Rx Termination Voltage	PWROK	weak pull-down 20kohm									
<div><p>R220 2 2.2K 4 1.8V_RUN</p><p>R221 2 1K_4 1</p><p>DF_TVS 25</p><p>H_SNB_IVB# 7</p></div>												

USB3.0

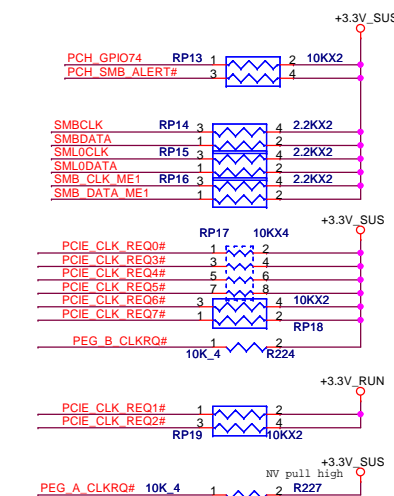
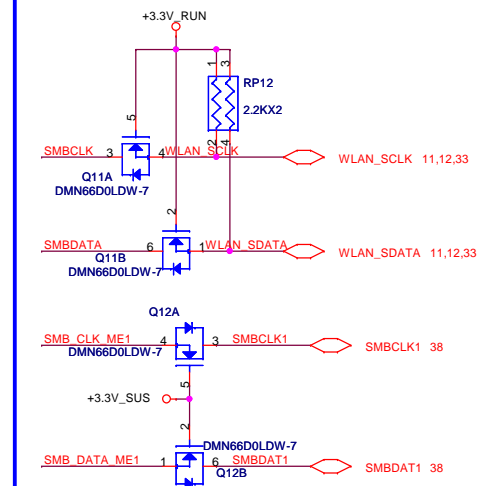


U14B Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)



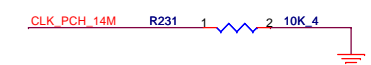
	Configurable as a GPIO or as a programmable output clock which can be configured as one of the following:
CLKOUTFLEX0 / GPIO64	• 33 / 27 / 48/ 14.318 MHz / DC Output logic '0'
CLKOUTFLEX1 / GPIO65	unsupported clock output value (Default) / 27/ 14.318 MHz output to SIO/EC / 48/24 MHz
CLKOUTFLEX2 / GPIO66	• 33/25/27/48/24/14.318 MHz / DC Output logic '0'
CLKOUTFLEX3 / GPIO67	• 27/14.318 output to SIO/48/24 MHz (Default)

SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)

Stuff for Integrated CLK Gen Mode

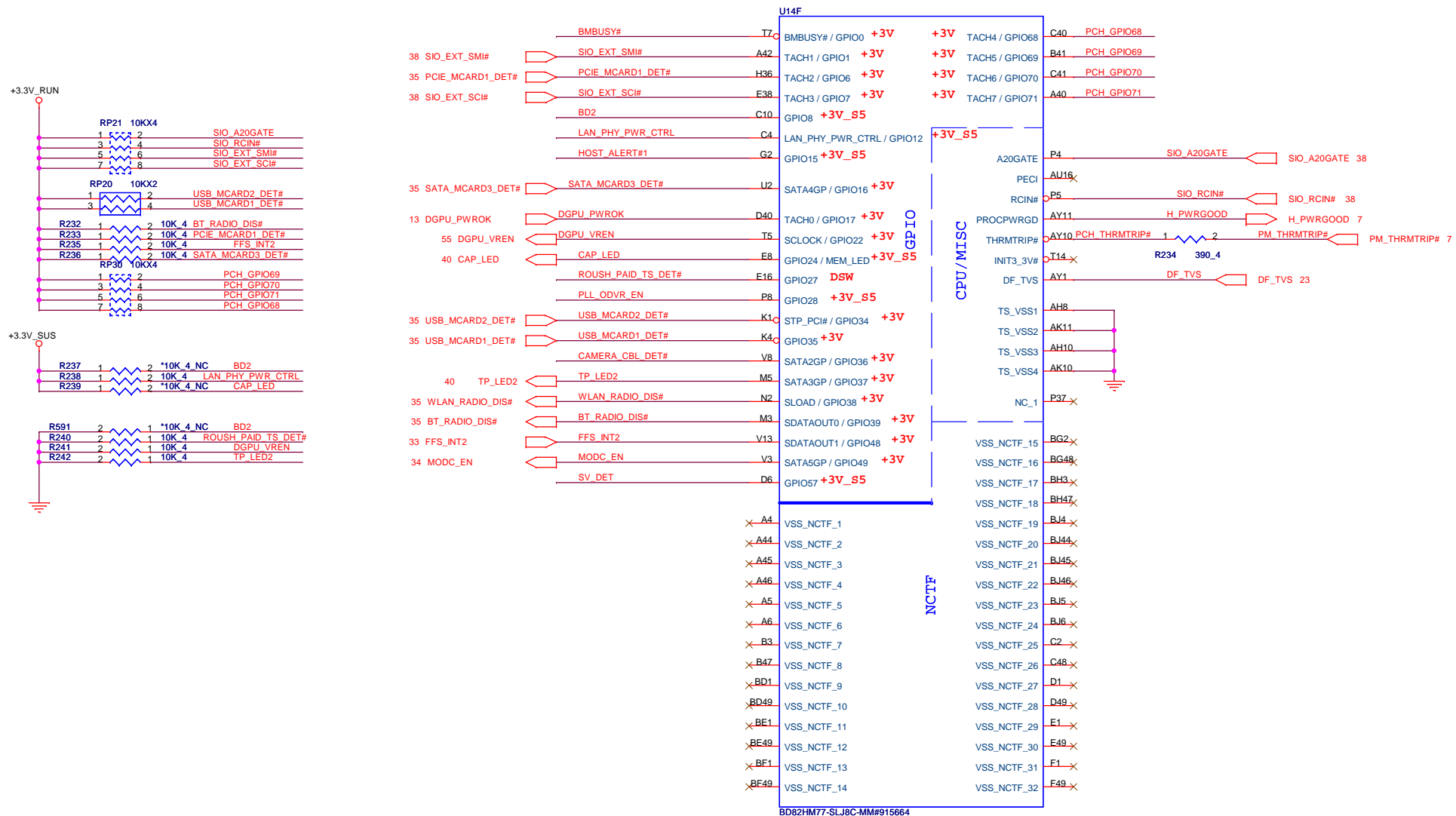
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Panther Point 5/7

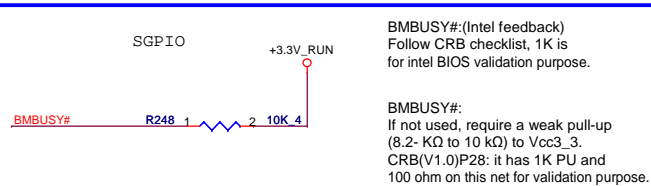
Size	Document Number	Rev
	Panther Point 5/7	1A
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Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)



Pin Name	Strap description	Sampled	Configuration
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)
-------------------------------------	--



HOST ALERT#1 R243 1 10K 4

SV_DET R245 1 10K 4

Intel ME Crypto Transport Layer
Security (TLS) cipher suite

Low = Disable (Default)
High = Enable

MFG-TEST

WLAN_RADIO_DIS# R249 1 10K 4
R250 1 10K 4

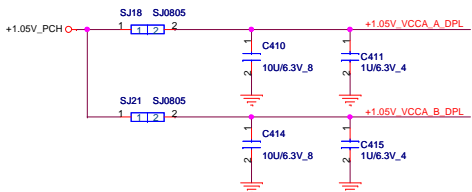
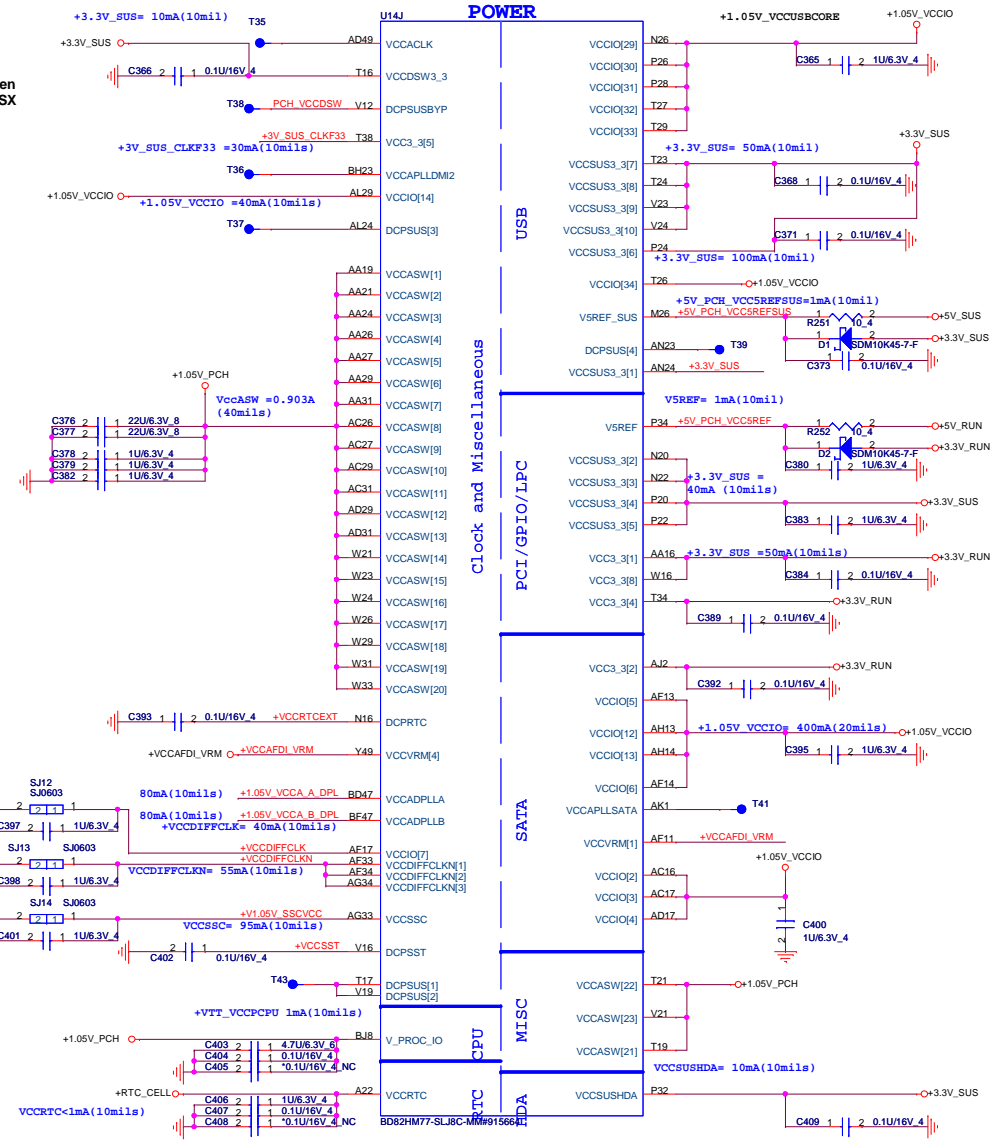
Quanta Computer Inc.

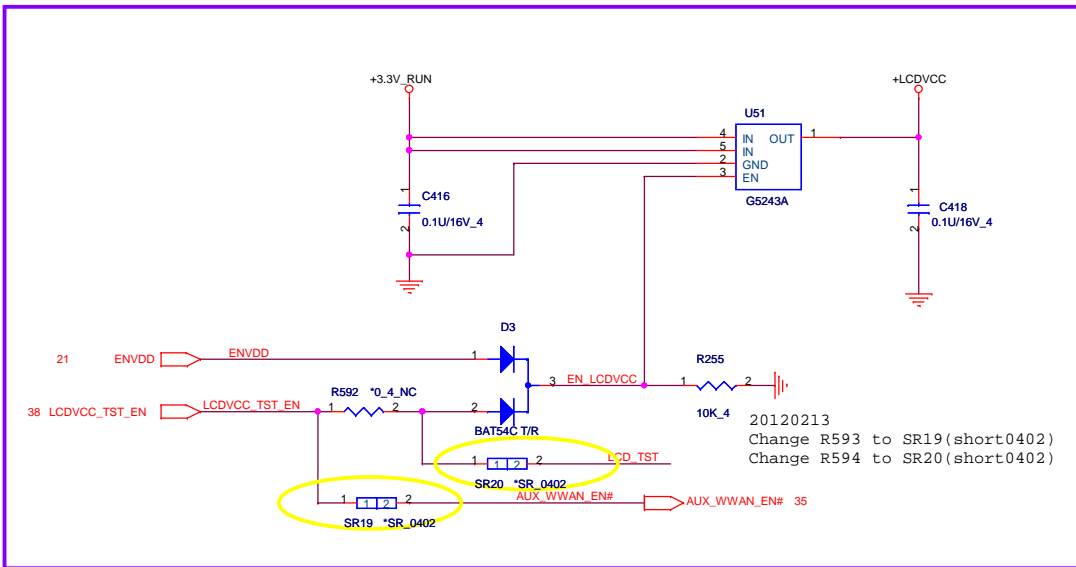
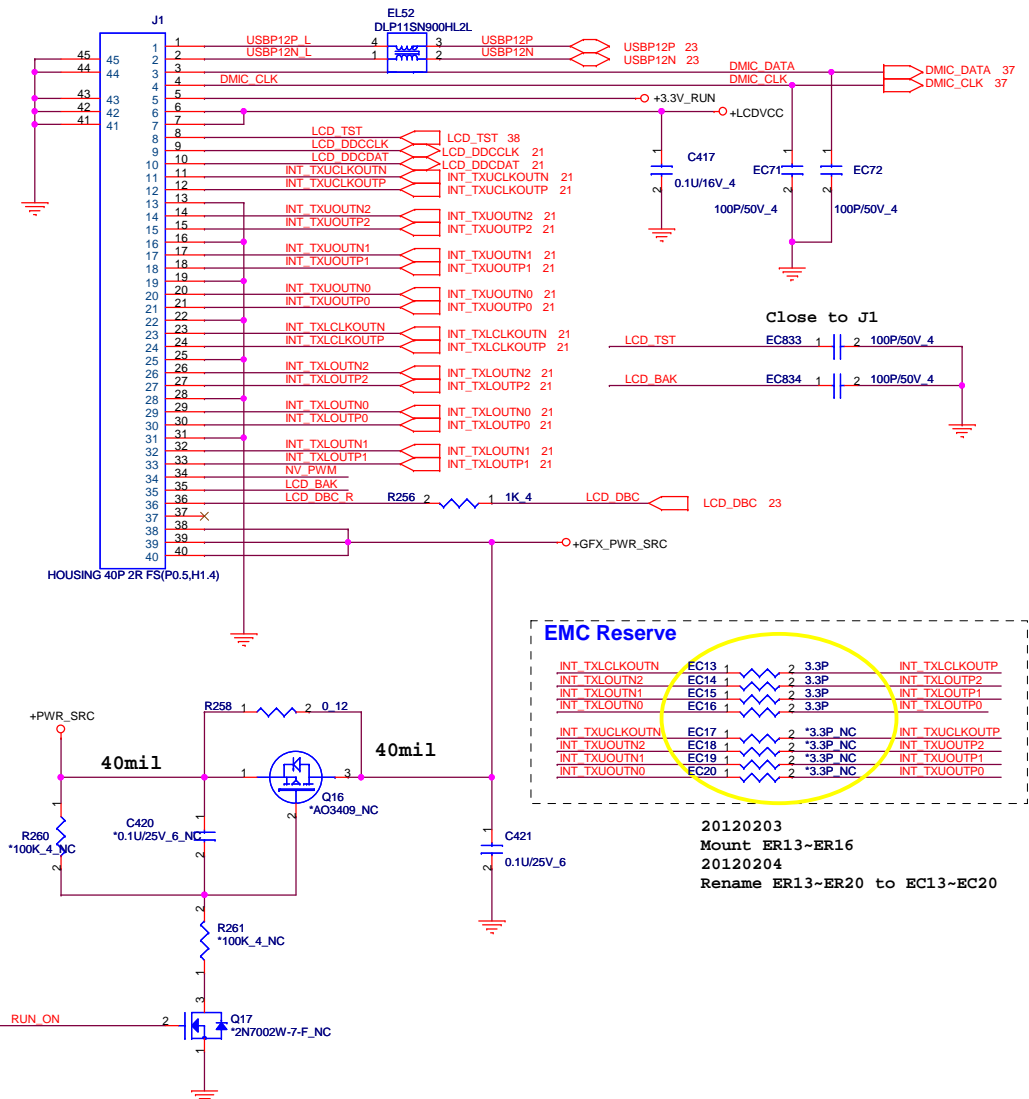
PROJECT : R08

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	Panther Point 6/7	1A

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Cougar Point/Panther Point (POWER)

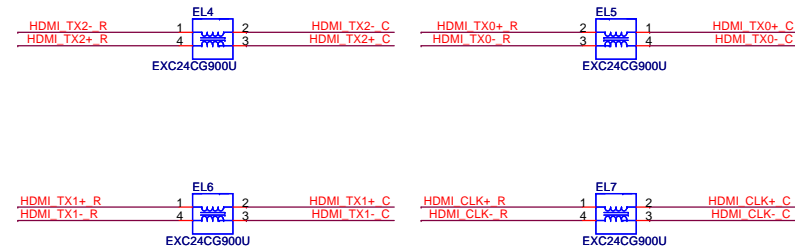


**Backlight Enable****Brightness Control**

HDMI

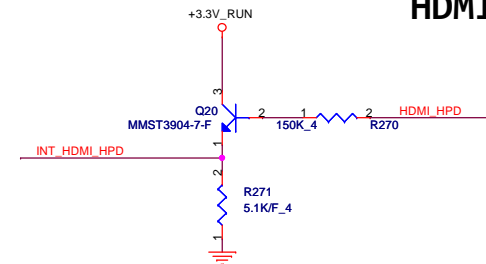
21 INT_HDMI_TXP2	INT_HDMI_TXP2	C425	1	2	0.1U/16V_4	HDMI TX2+ R
21 INT_HDMI_TXN2	INT_HDMI_TXN2	C426	1	2	0.1U/16V_4	HDMI TX2- R
21 INT_HDMI_TXP1	INT_HDMI_TXP1	C427	1	2	0.1U/16V_4	HDMI TX1+ R
21 INT_HDMI_TXN1	INT_HDMI_TXN1	C428	1	2	0.1U/16V_4	HDMI TX1- R
21 INT_HDMI_TXP0	INT_HDMI_TXP0	C429	1	2	0.1U/16V_4	HDMI TX0+ R
21 INT_HDMI_TXN0	INT_HDMI_TXN0	C430	1	2	0.1U/16V_4	HDMI TX0- R
21 INT_HDMI_TXCP	INT_HDMI_TXCP	C431	1	2	0.1U/16V_4	HDMI CLK+ R
21 INT_HDMI_TXCN	INT_HDMI_TXCN	C432	1	2	0.1U/16V_4	HDMI CLK- R
21 HDMI_SCL	HDMI_SCL					
21 HDMI_SDA	HDMI_SDA					
21 INT_HDMI_HPD	INT_HDMI_HPD					

Reserve for EMI and close to HDMI CONN



HDMI_HPD spec VinH_min=2.0V

HDMI HPD

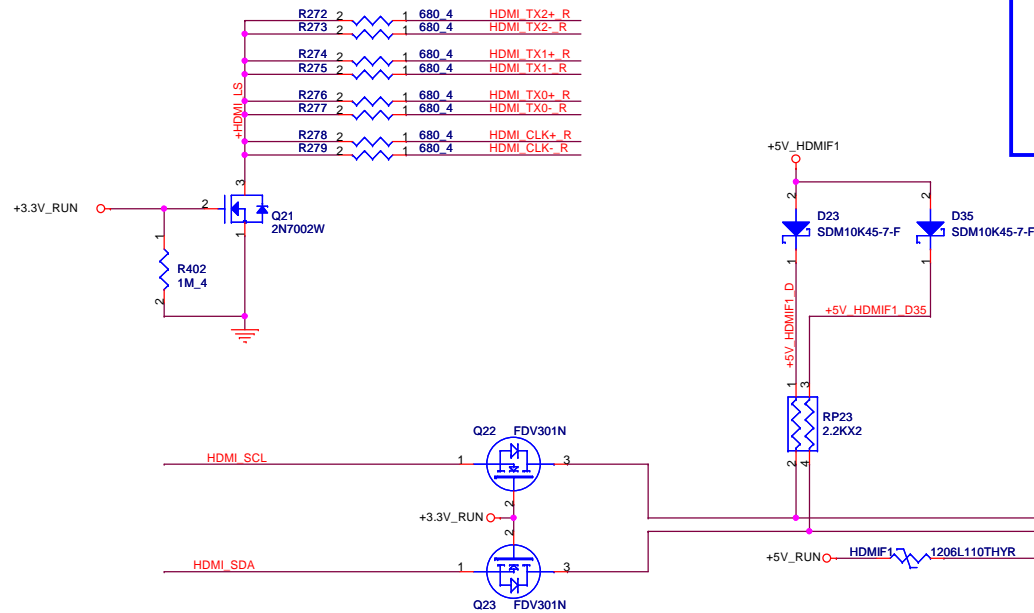


$$IB = (5V - 0.7V) / (150K + (70 + 1) 5.1K) = 8.4\mu A$$

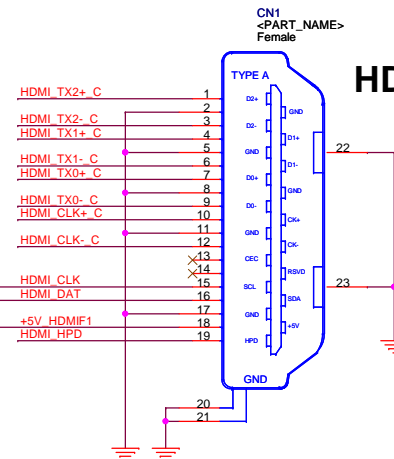
$$IE = (1 + 70) \times 8.4\mu A = 596.4\mu A$$

$$VE = 596.4\mu A \times 5.1K = 3.04V$$

$$B = 70$$



HDMI Conn.



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	A	B	C	D	E
4					
3					
2					
1					



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PROJECT : R08

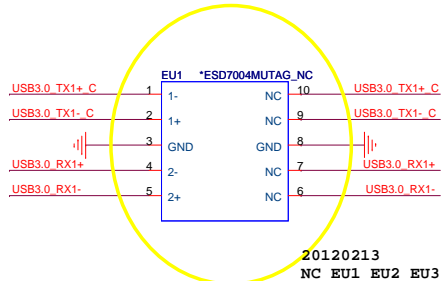
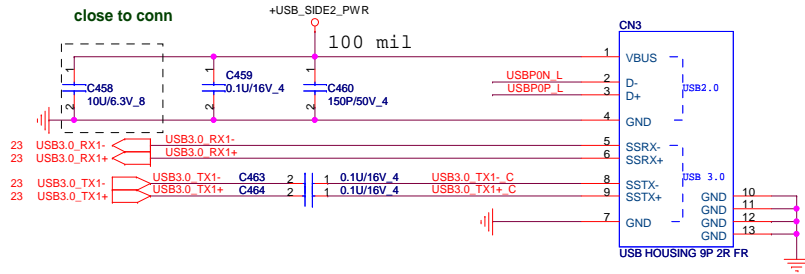
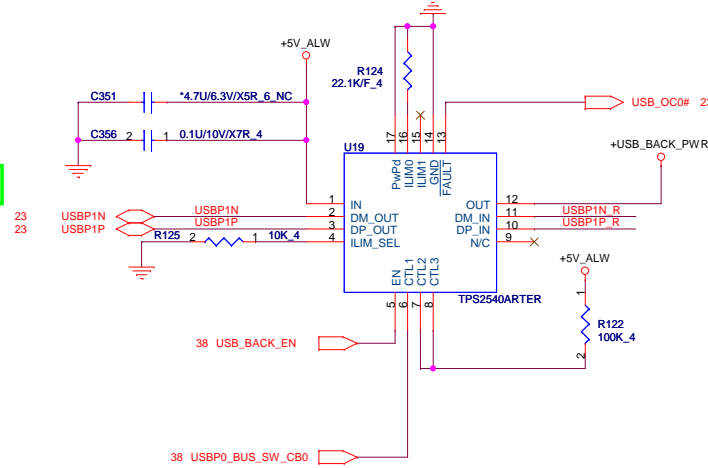
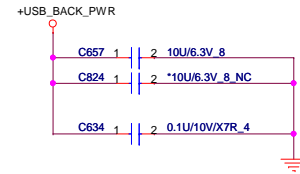
Size	Document Number	Rev
	NA	1A
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USB Power share

USBP0_BUS_SW_CB0	Mode	Operating at
Low	DCP, Auto-detect	S3/S4/S5, 1.5 A
High	CDP, BC Spec 1.1	S0, 1.5 A

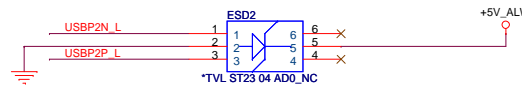
	R109	mA
OC limitation	100k ohm	480
	22.1k ohm	2171

Applied Now

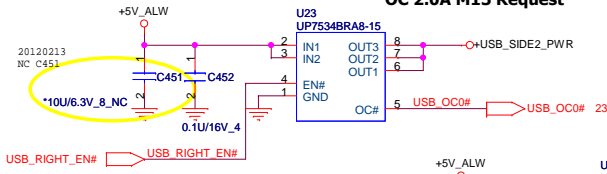


ESD Function

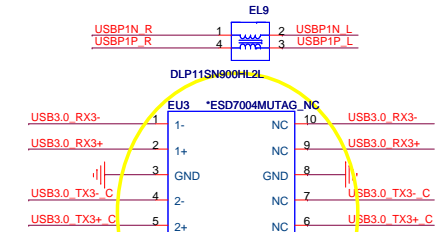
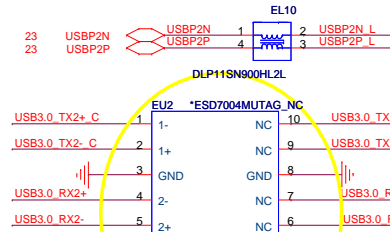
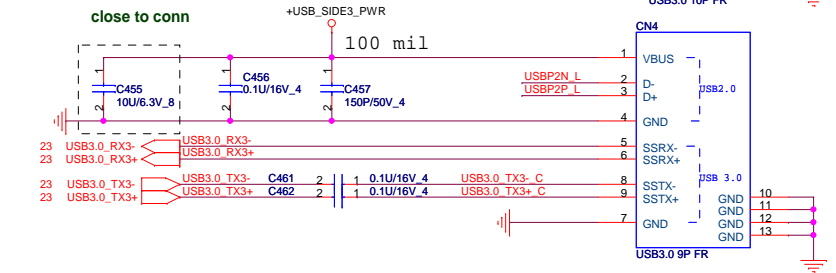
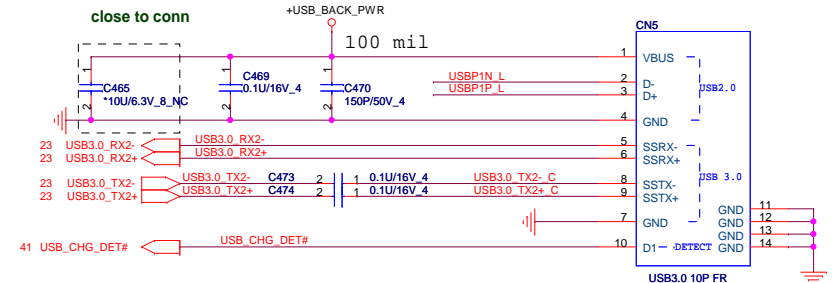
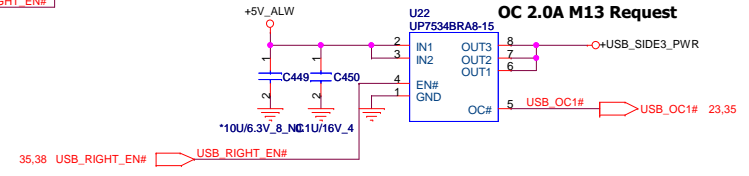
Place ESD diodes as close as USB connector.



I continuous 1.5A OC 2.0A M13 Request



I continuous 1.5A OC 2.0A M13 Request



ESD Function



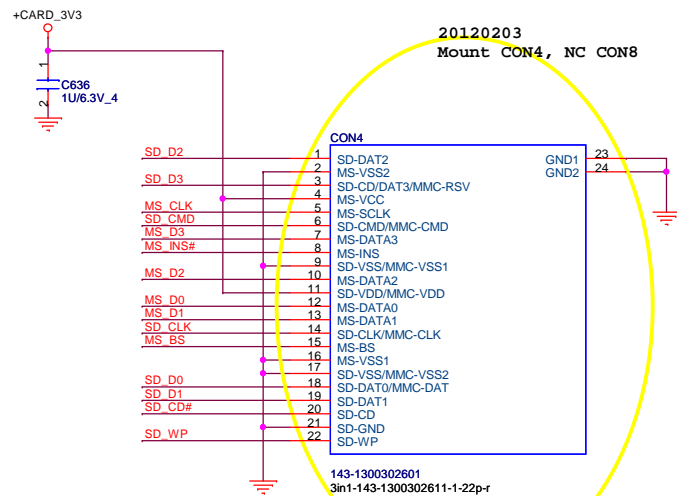
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PROJECT : R08

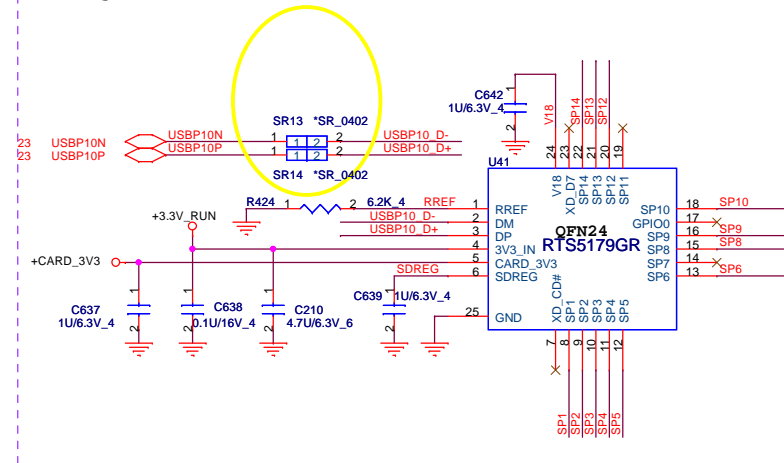
Size	Document Number	Rev
	USB 3.0 port / USB power share	1A
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Cardreader (RTS5179GR) Support SD3.0 USH50

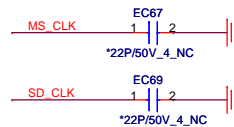
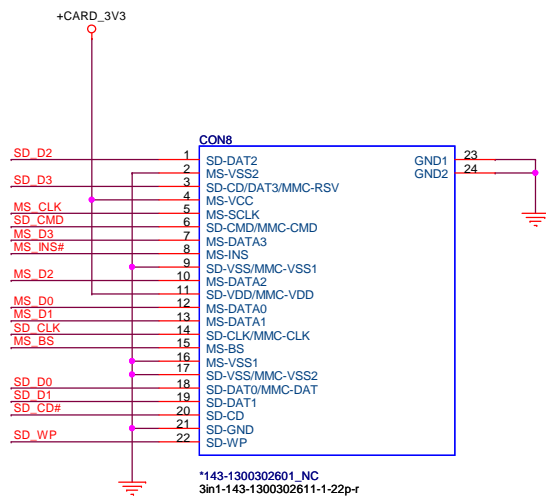
For Vostro Placement(V08,V08A)-Far ODD



20120206
Remove EL47
Change R210 to SR13(short0402)
Change R212 to SR14(short0402)



For INSPIRON Placement (R08,R08A,R08T)-Near ODD



SP1	SD_WP	MS_CLK
SP2	SD_D1	MS_INS#
SP3	SD_D0	MS_D7
SP4	SD_D7	MS_D3
SP5	SD_CD#	
SP6		
SP8	SD_CLK	MS_D2
SP9	SD_D5	MS_D0
SP10	SD_CMD	
SP12	SD_D3	MS_D1
SP13	SD_D2	MS_D5
SP14		MS_BS

Share Pin

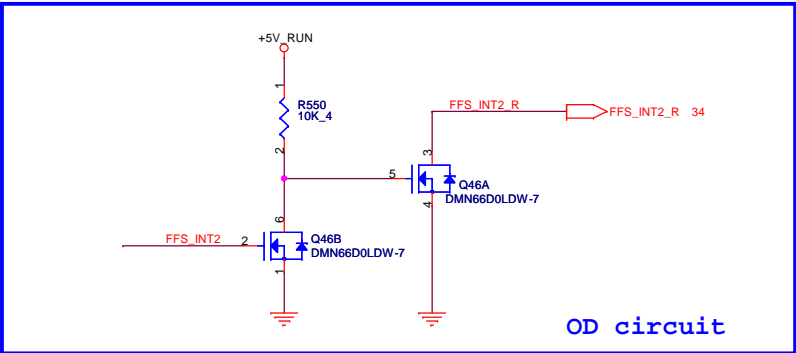


Quanta Computer Inc.
PROJECT : R08

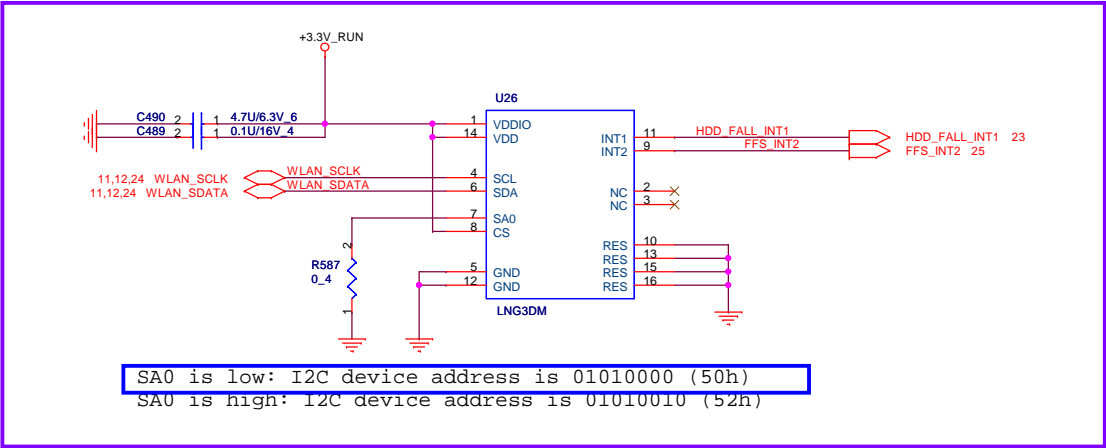
Size	Document Number	Rev
	Cardreader (RTS5179GR)	1A
Date	Monday, February 13, 2012	Sheet 32 of 55

3-axis Fall Sensor

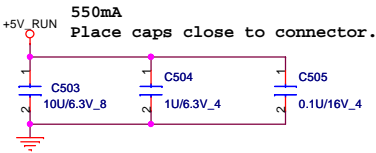
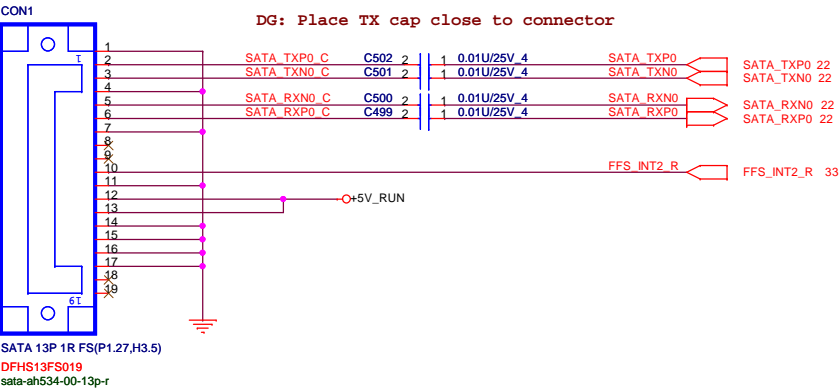
If you have two HDD,need add two OD circuit for Fall sensor interrupt circuit



20120203
Mount Function code "FFS" part

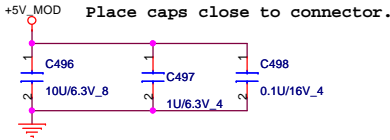
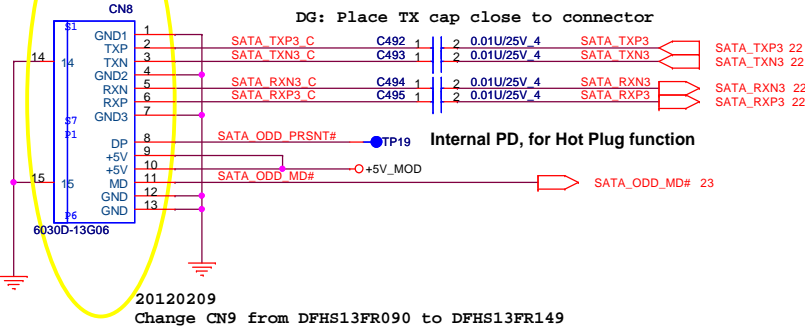


HDD

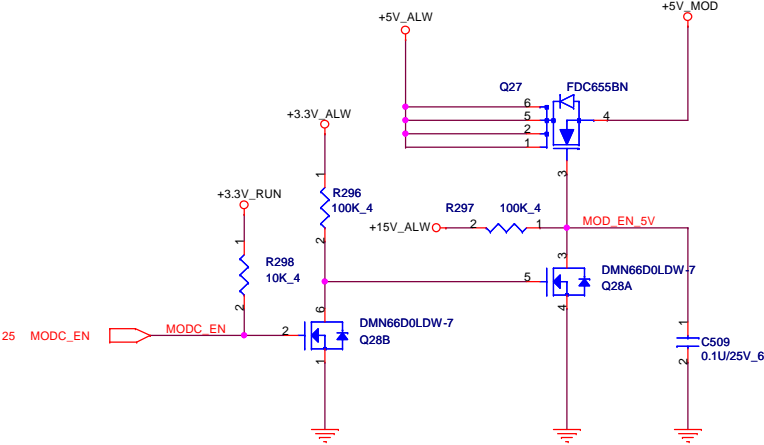


ODD

ODD Connector



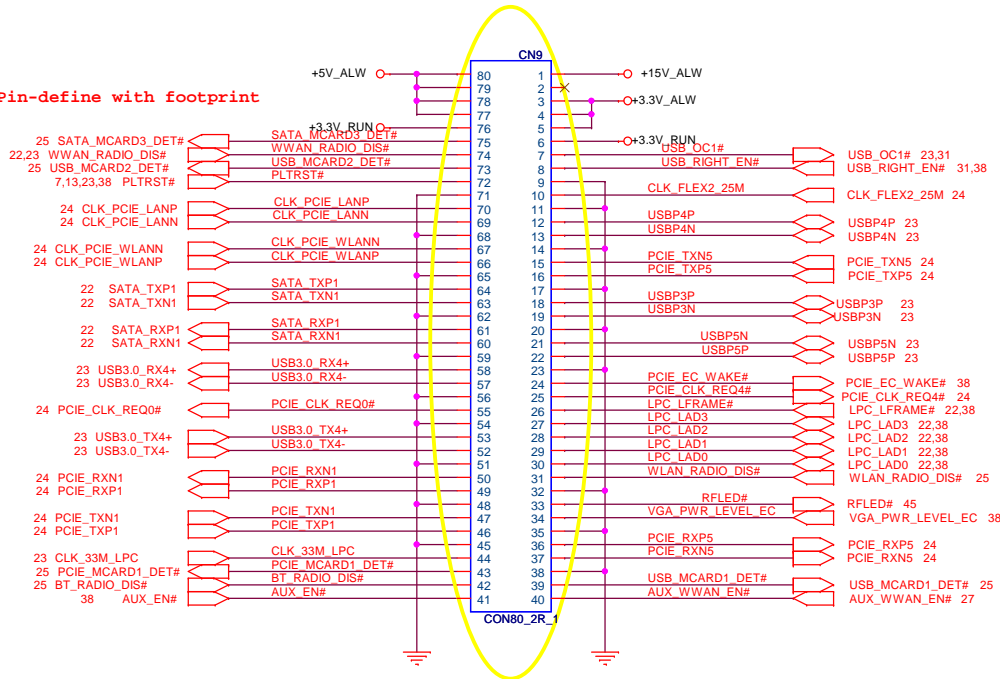
Support Zero power ODD



20120203

Change CN9 footprint from "88069-8001b-bs-80p-ldh" to "88069-8001b-bs-80p-ldh-smt"

Check Pin-define with footprint

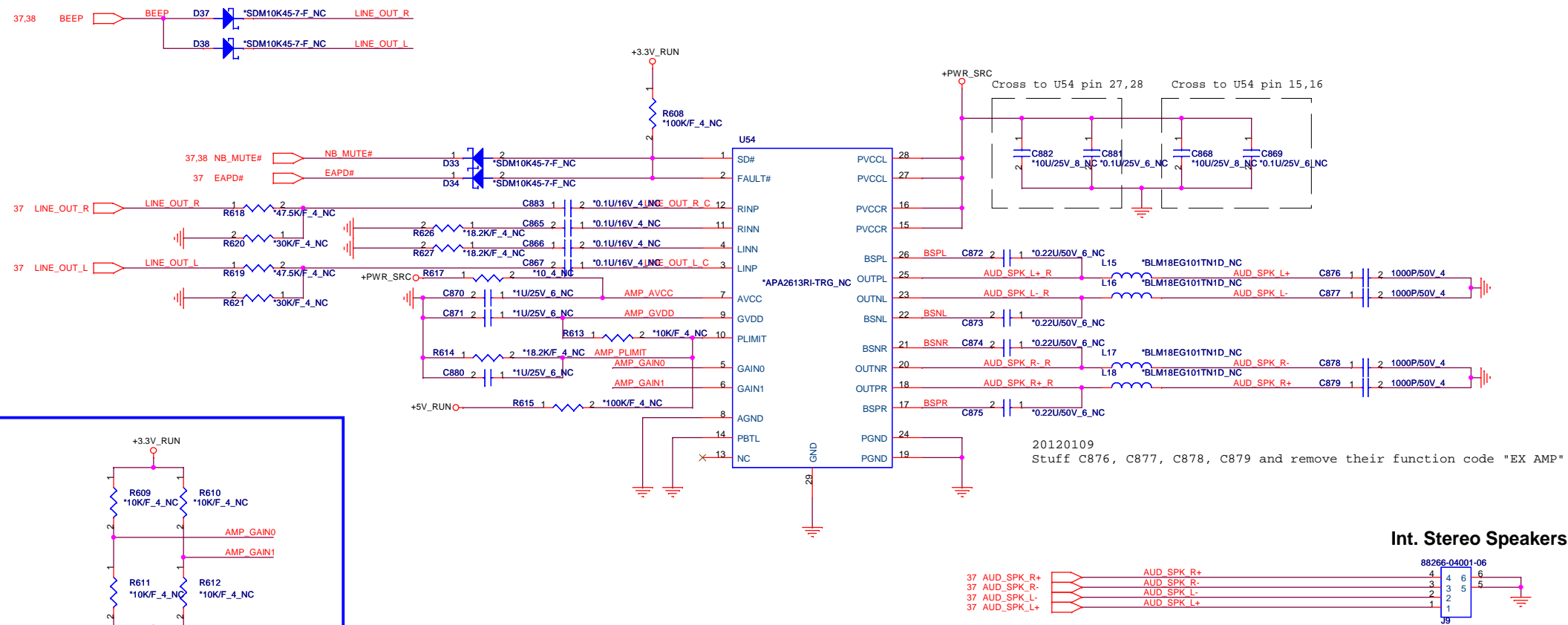


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	BTB CONN	3A
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ANPEC APA2613 is P2P to TI TPA3113 Default use APA2613

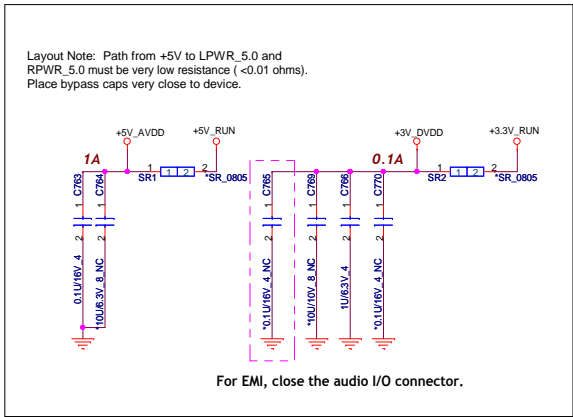
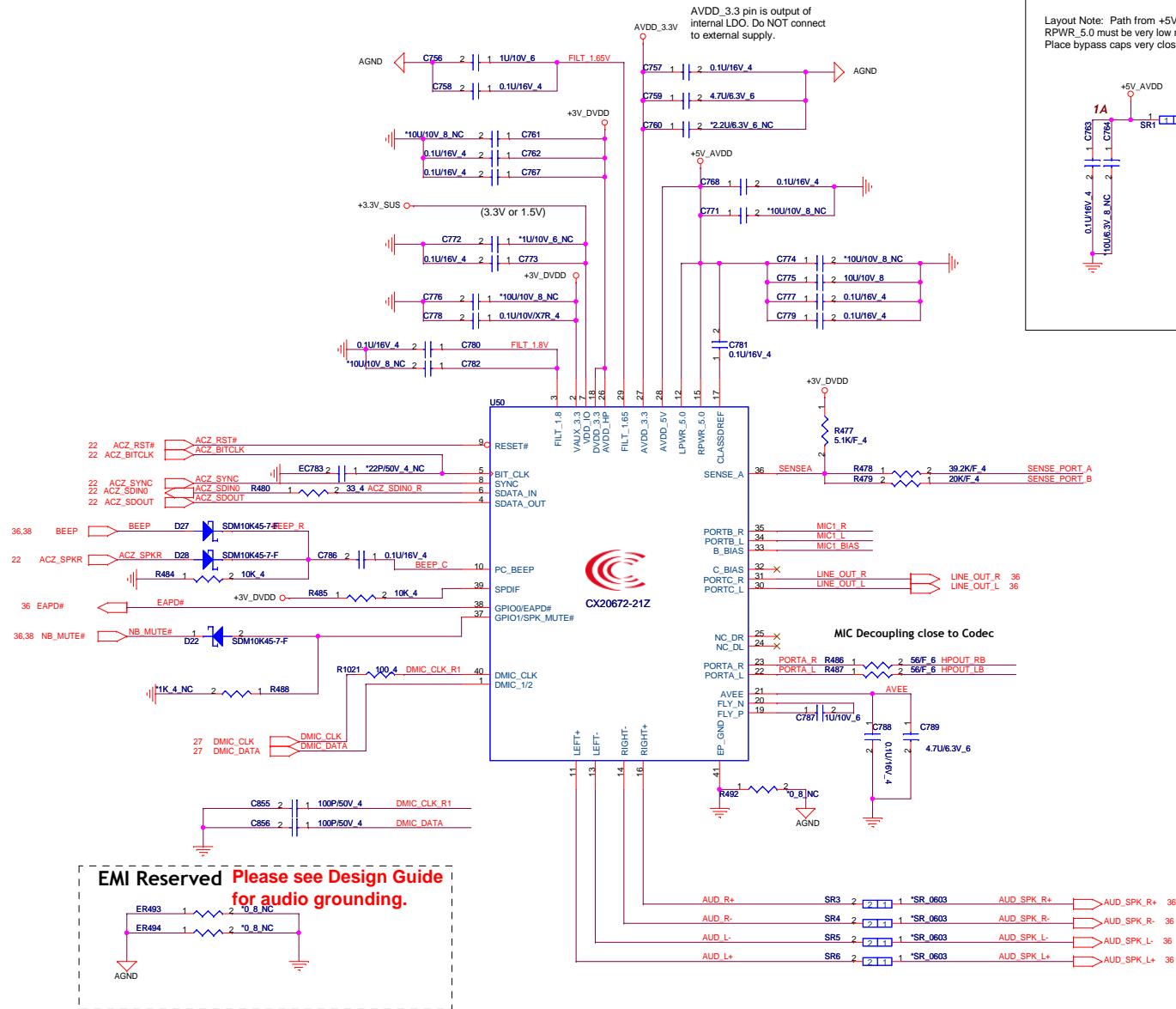


Int. Stereo Speakers

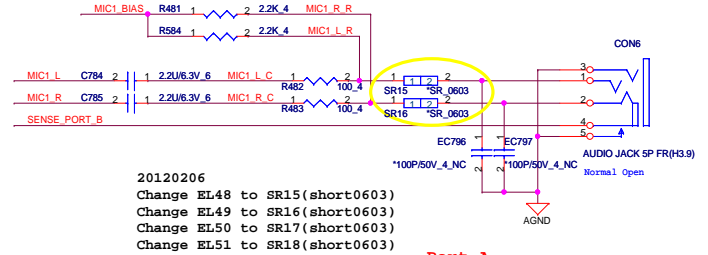


GAIN1	GAIN0	AMPLIFIER GAIN (dB)	
		TYP	
0	0	20	
0	1	26	
1	0	32	
1	1	36	

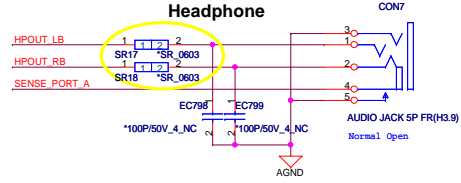
	Amplifier	Function code
R08/R08A/V08/V08A	CODEC CX20672	Mount "IN AMP"
R08T	APA2613 or TPA3113	Mount "EX AMP"



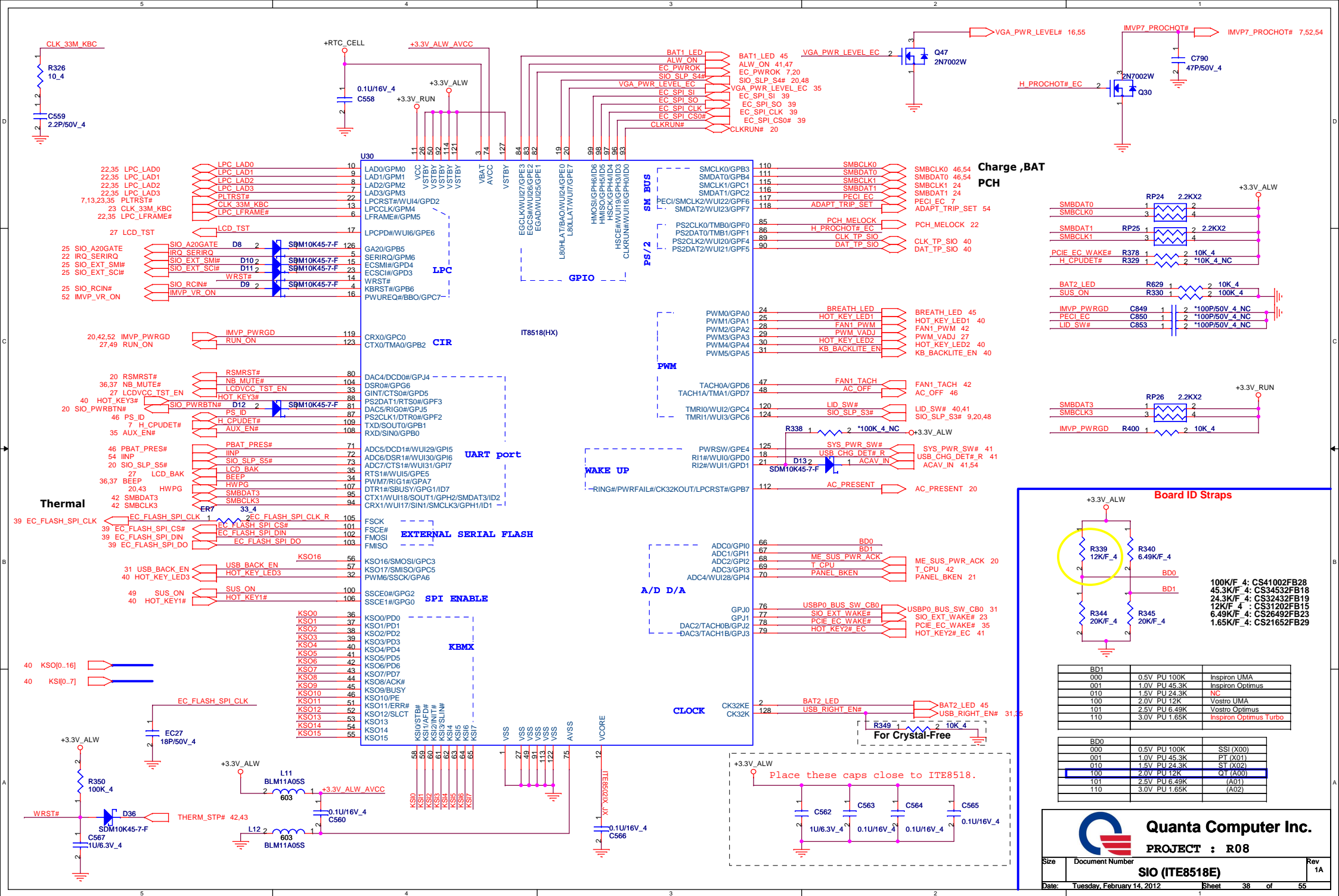
Port B
External Stereo microphone



Port A
Headphone

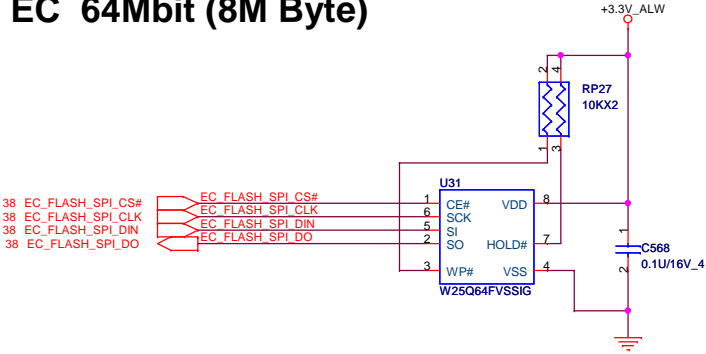


Flow PDC pin define

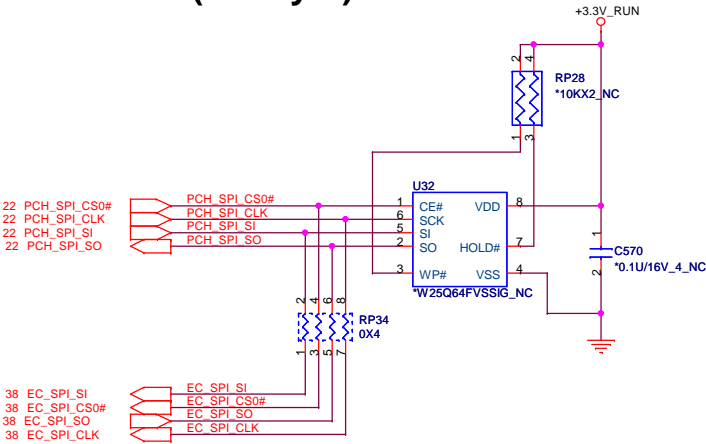


FLASH / RTC

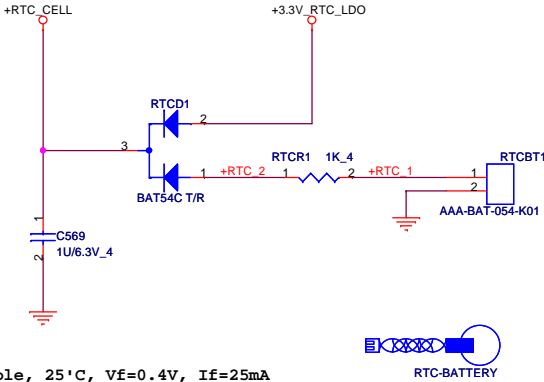
For EC 64Mbit (8M Byte)



For PCH 64Mbit (8M Byte)

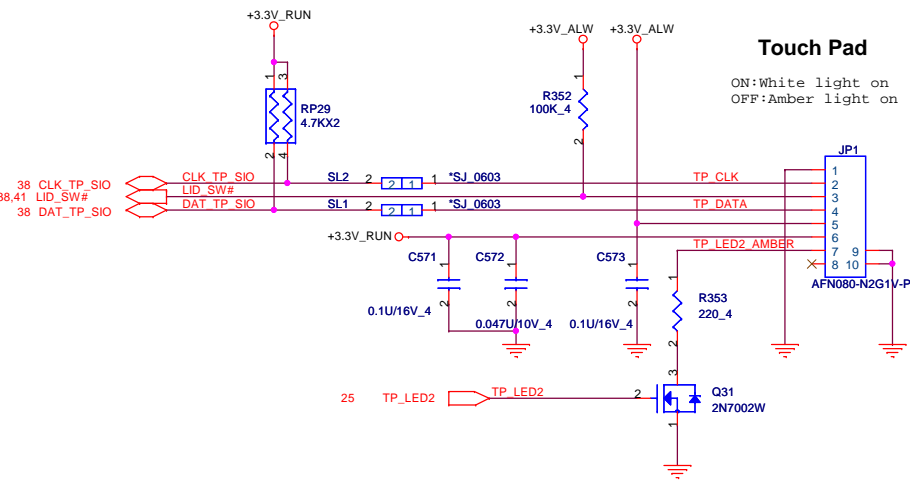


RTC

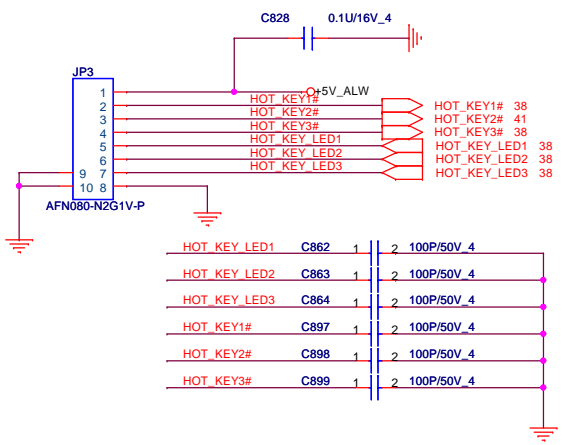


Double, 25°C, Vf=0.4V, If=25mA
one, 25°C, Vf=0.35V, If=15.8mA

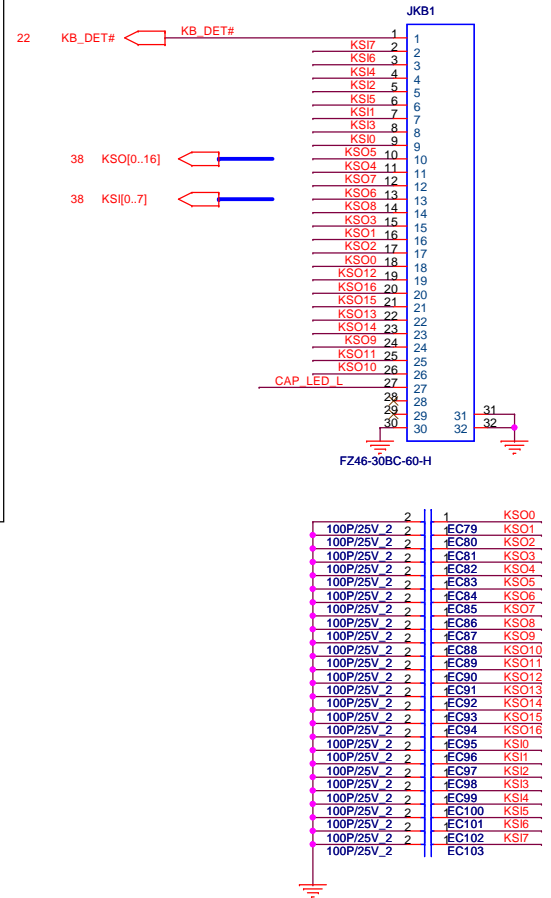
TP CONNECTOR



HotKey CONN

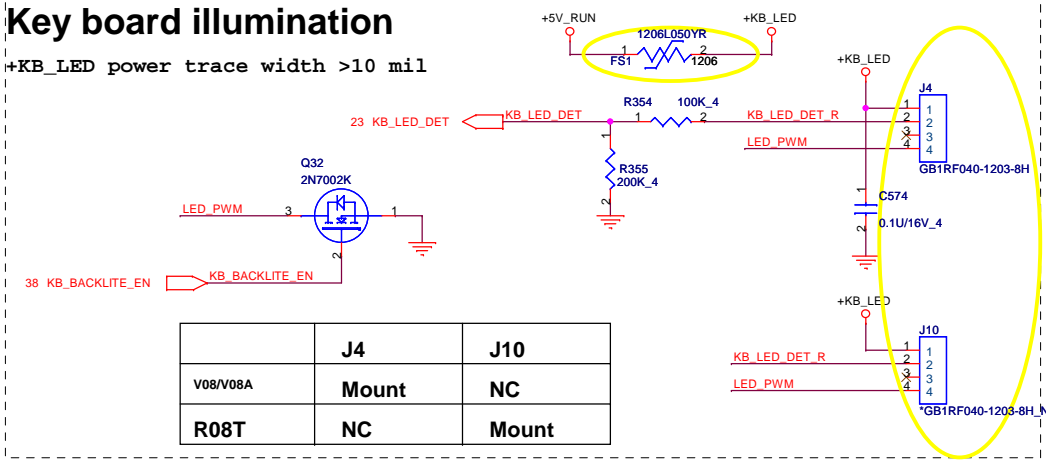


KB CONN



Key board illumination

+KB_LED power trace width >10 mil

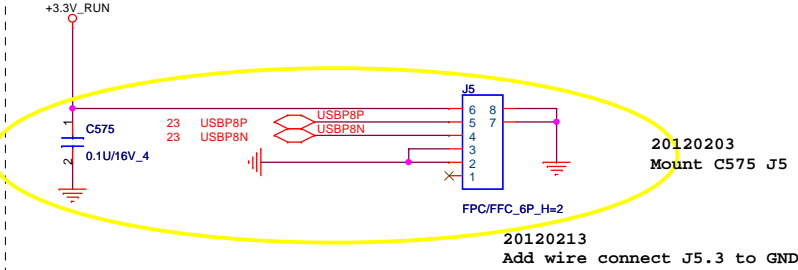


20120206
Change FS1 to SR12(short1206)
20120213
Change SR12 back to FS1

20120203
Mount J4, NC J10

	J4	J10
V08/V08A	Mount	NC
R08T	NC	Mount

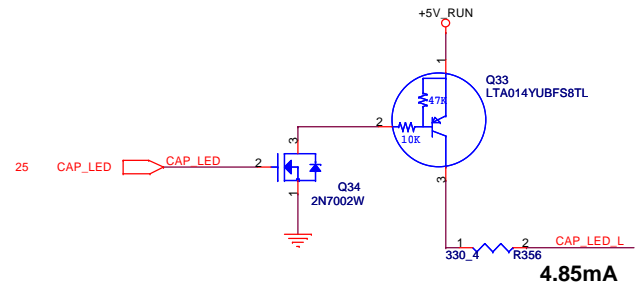
Fingerprint



20120203
Mount C575 J5

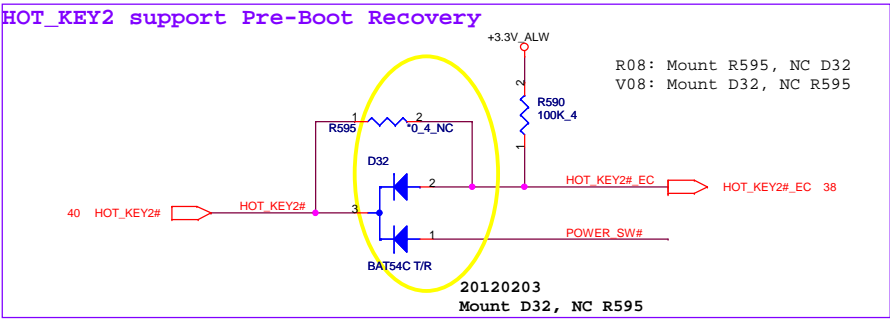
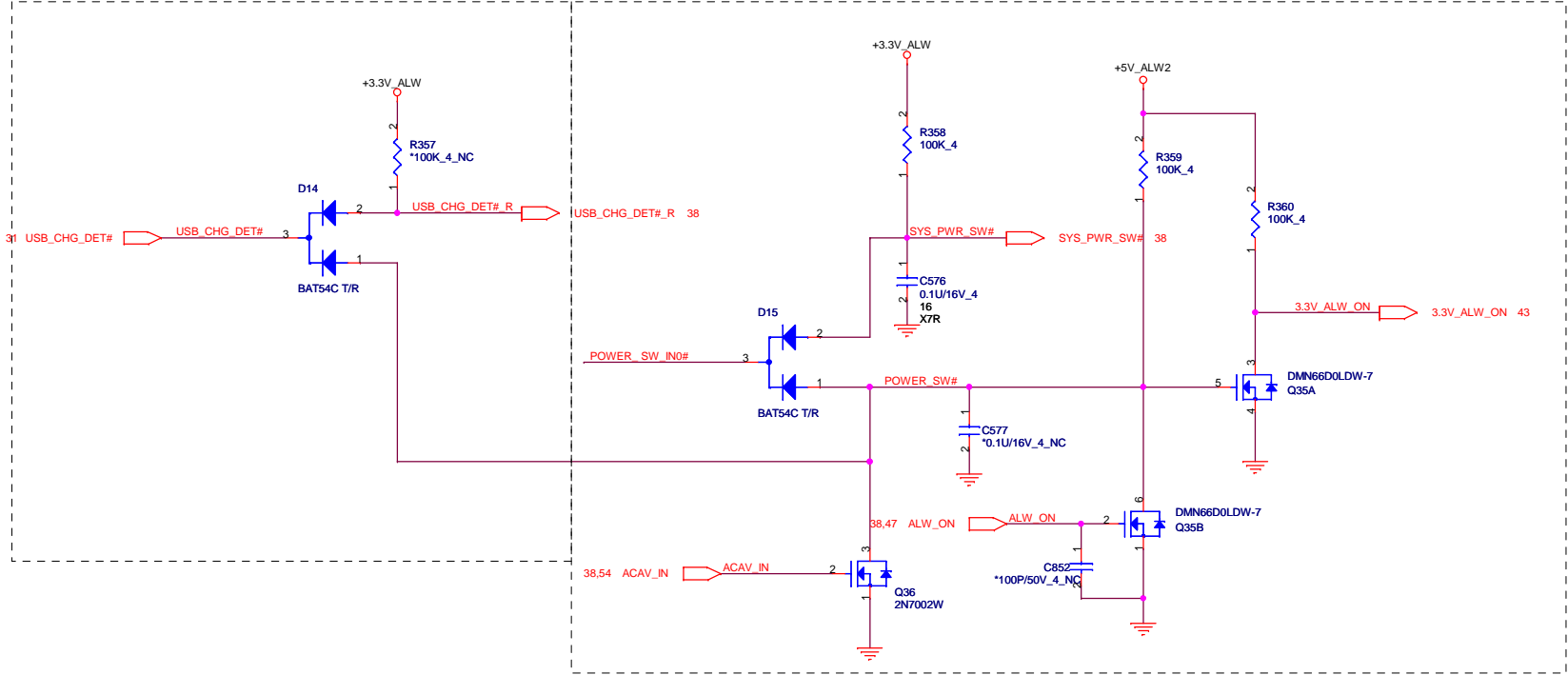
20120213
Add wire connect J5.3 to GND

Vi(on_max)= -1.4V
Vi(off_min)=-0.3

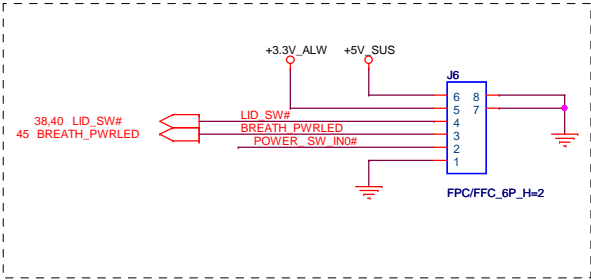


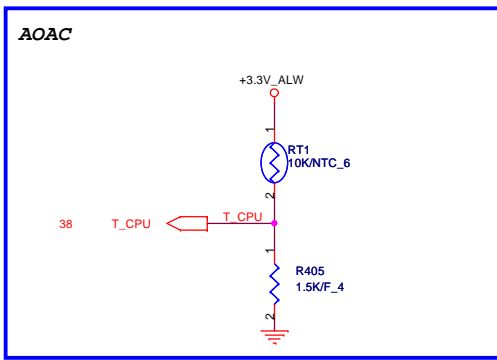
For USB charger usage

3V ALW ON POWER LOGIC



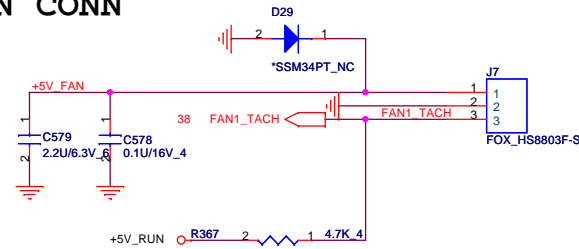
TO PWR button board





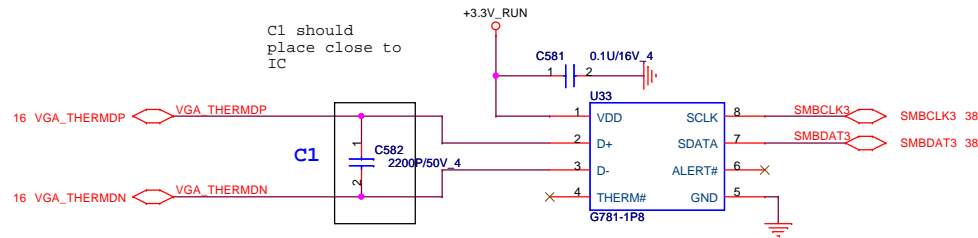
20120203
Mount RT1 R405 for V08A SKU

FAN CONN



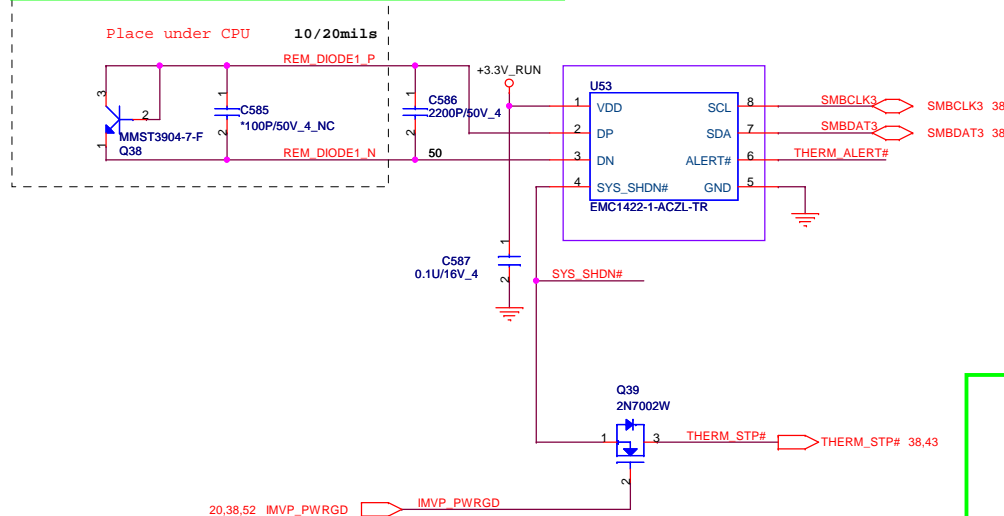
G781-1P8

SMBus address is 1001101xb (9Ah) (x is R/W bit).



THERMAL IC

1. Place C586 close to EMC1422-U1
 2. Place C585 to be close to Q38
- Total capacitance between D+/D- is 2200pF(max)
if use 2200pF for C586, then C585 should be dummy

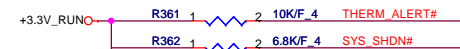


EMC1422 SMBus address is 1001_100xb (98h) (x is R/W bit).

SYS_SHD#	4.7K	6.8K	10K	15K	22K	33K
ALERT#	4.7K	77°C	83°C	89°C	95°C	101°C
6.8K	78°C	84°C	90°C	96°C	102°C	108°C
10K	79°C	85°C	91°C	97°C	103°C	109°C
15K	80°C	86°C	92°C	98°C	104°C	110°C
22K	81°C	87°C	93°C	99°C	105°C	111°C
33K	82°C	88°C	94°C	100°C	106°C	112°C

CHECK OTP WITH Thermal.

OTP 85 degree C



EMC1422

OTP 85 degree : R361 = 10K, R362 = 6.8K
OTP 90 degree : R361 = 6.8K, R362 = 10K

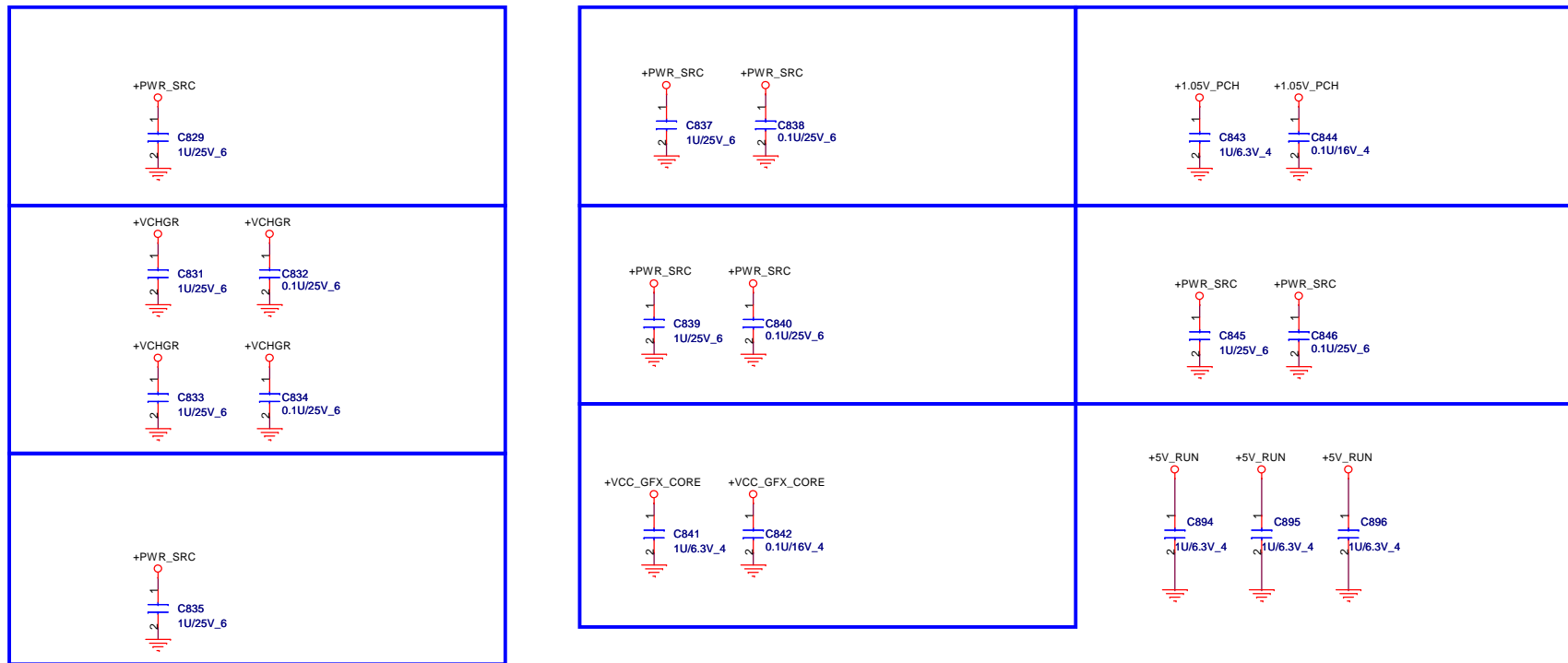
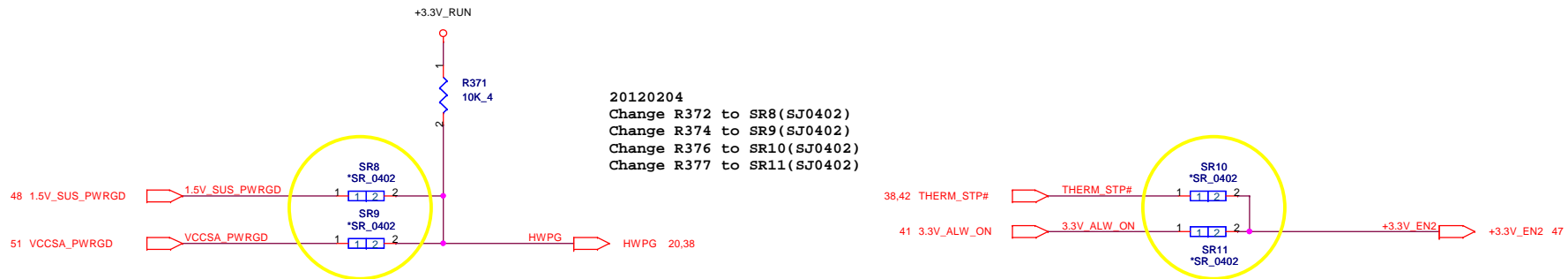
NTC7718W

OTP 85 degree : R361 = 18.7K, R362 = 2K
OTP 91 degree : R361 = 10.5K, R362 = 7.5K

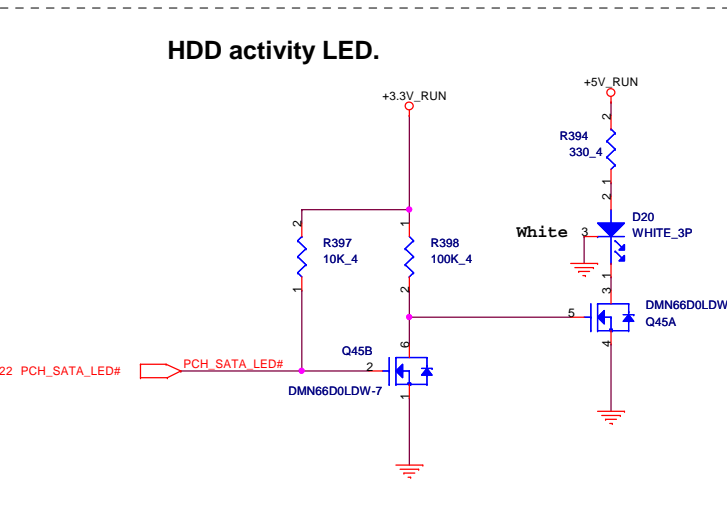
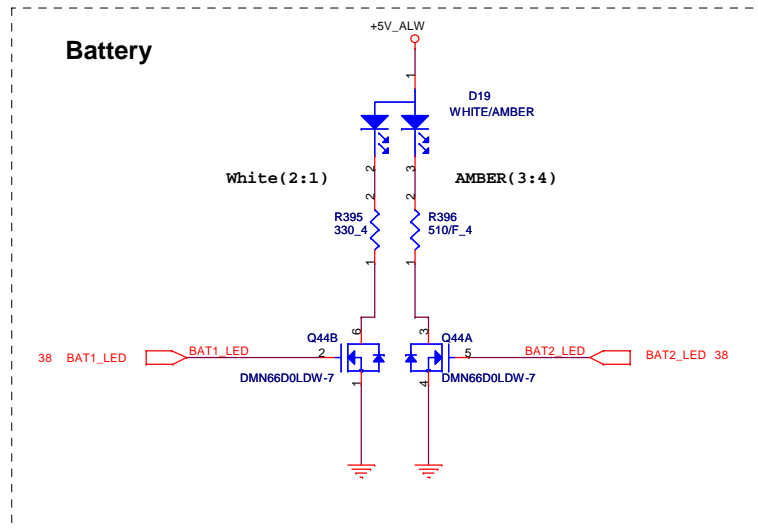
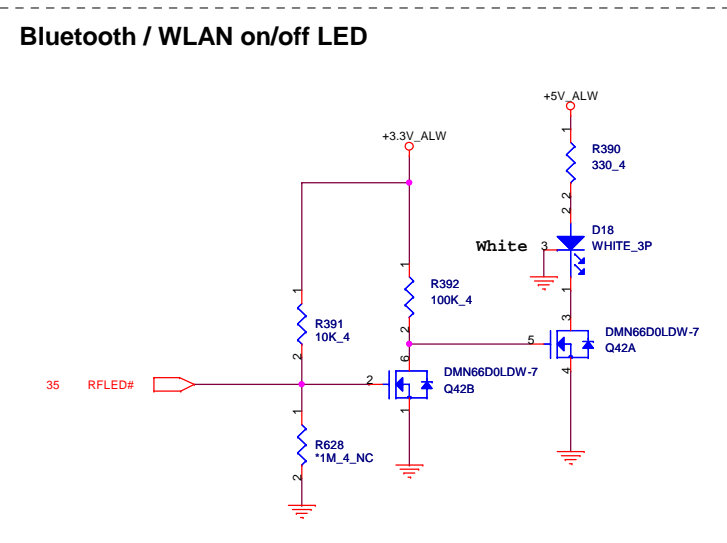
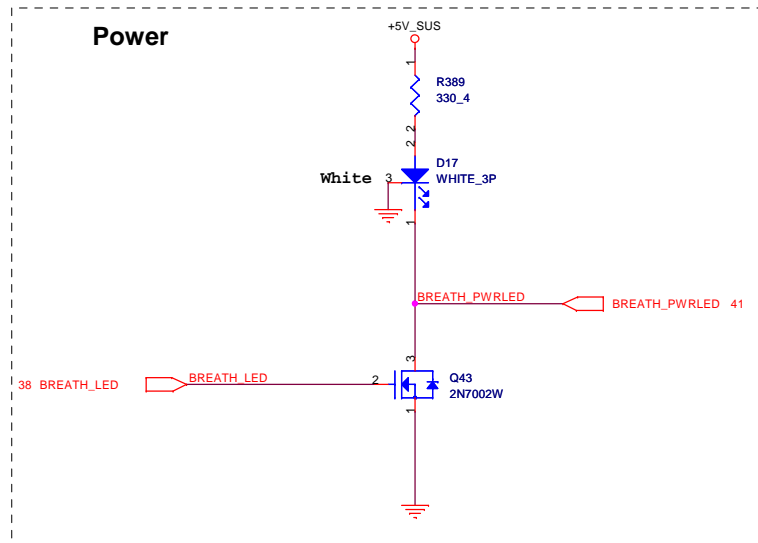


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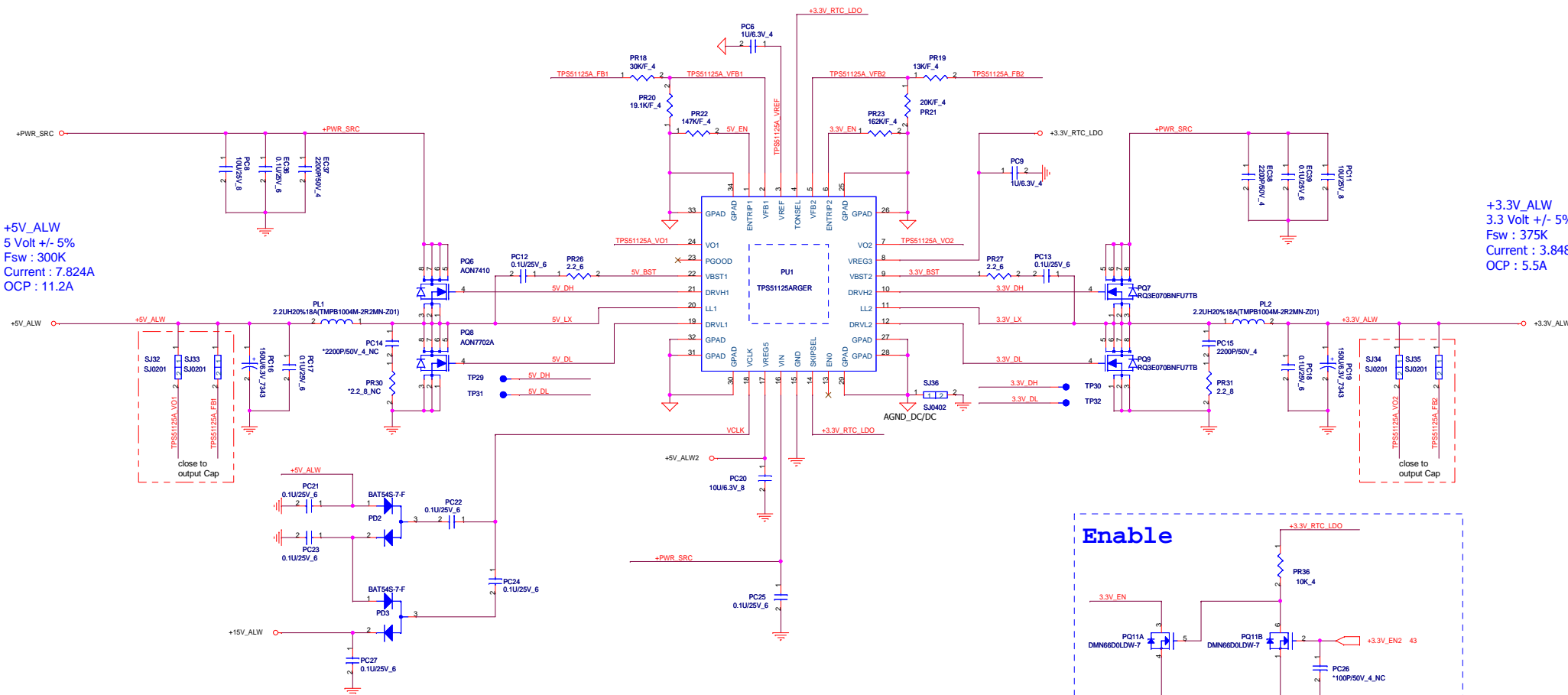




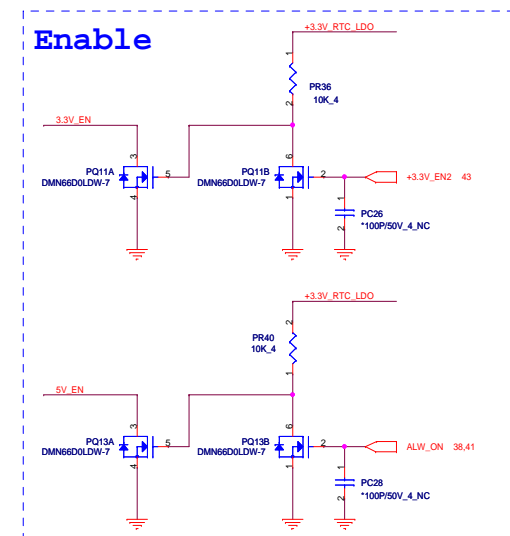


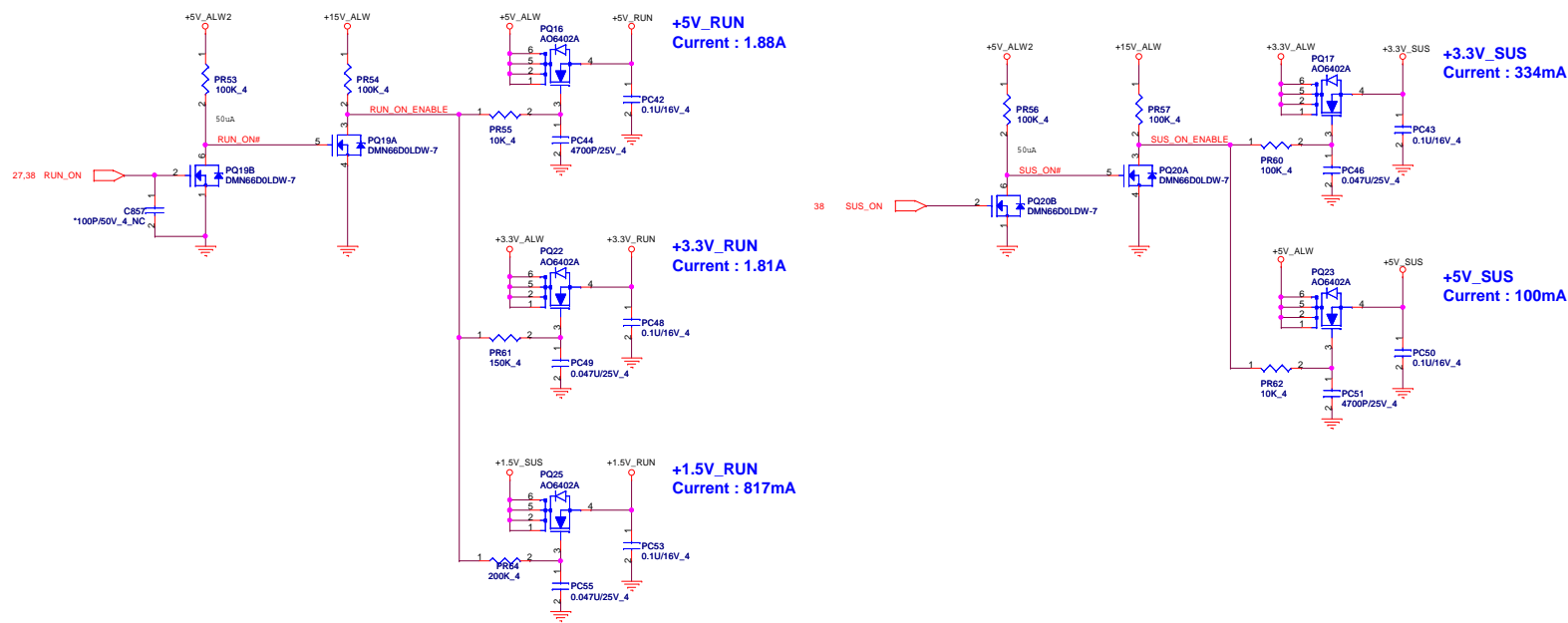
+5V_ALW
5 Volt +/- 5%
Fsw : 300K
Current : 7.824A
OCP : 11.2A

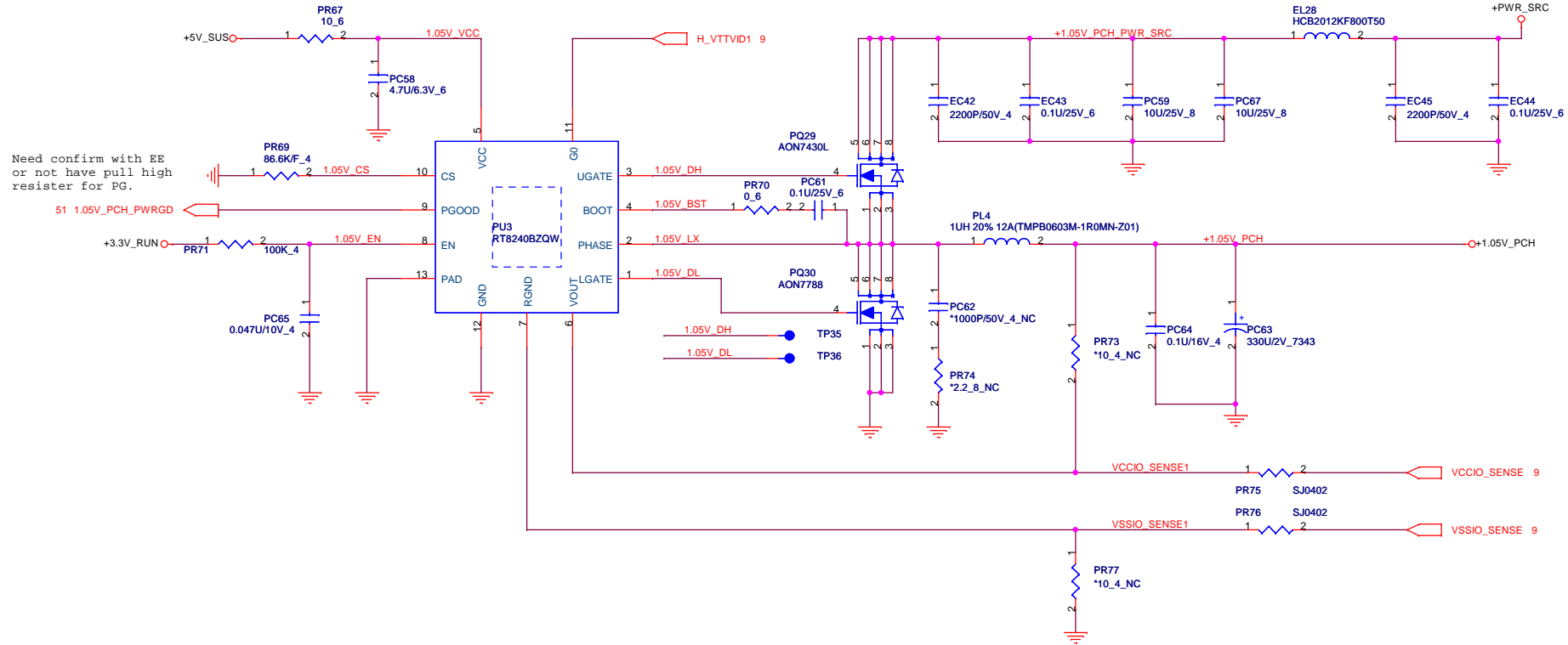
+3.3V_ALW
3.3 Volt +/- 5%
Fsw : 375K
Current : 3.848A
OCP : 5.5A



TPS51125A TONSEL Connection and Switching Frequency				
Ton	REG5	REG3	VREF	GND
Channel1 Fs	365 kHz	300 kHz	245 kHz	200 kHz
Channel2 Fs	460 kHz	375 kHz	305 kHz	250 kHz







+1.05V_PCH
1.05 Volt DC +/- 2%
Fsw : 400K
TDC : 13.5A
OCP : 19.5A

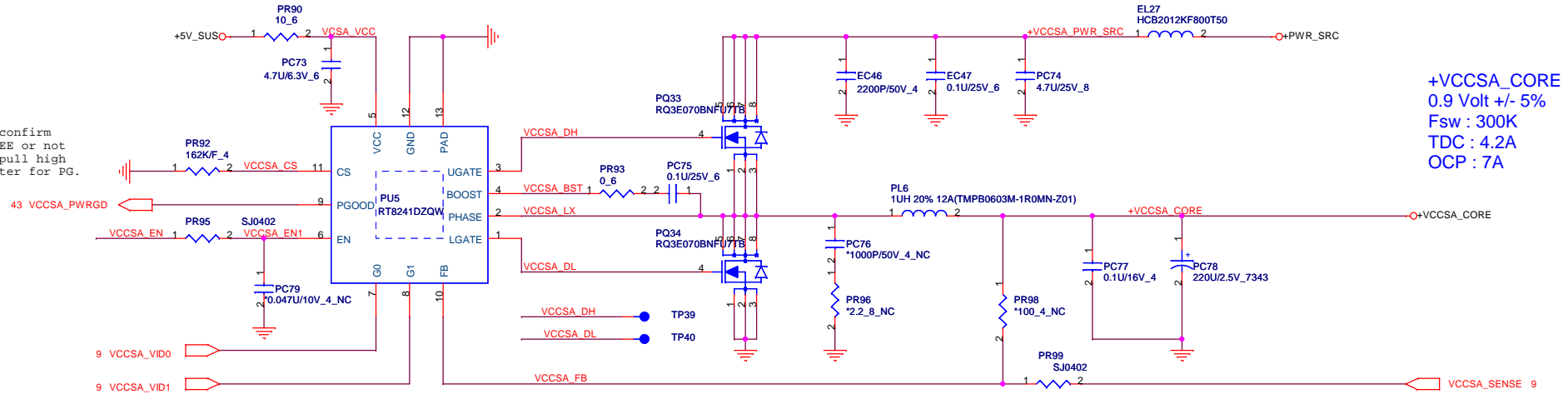


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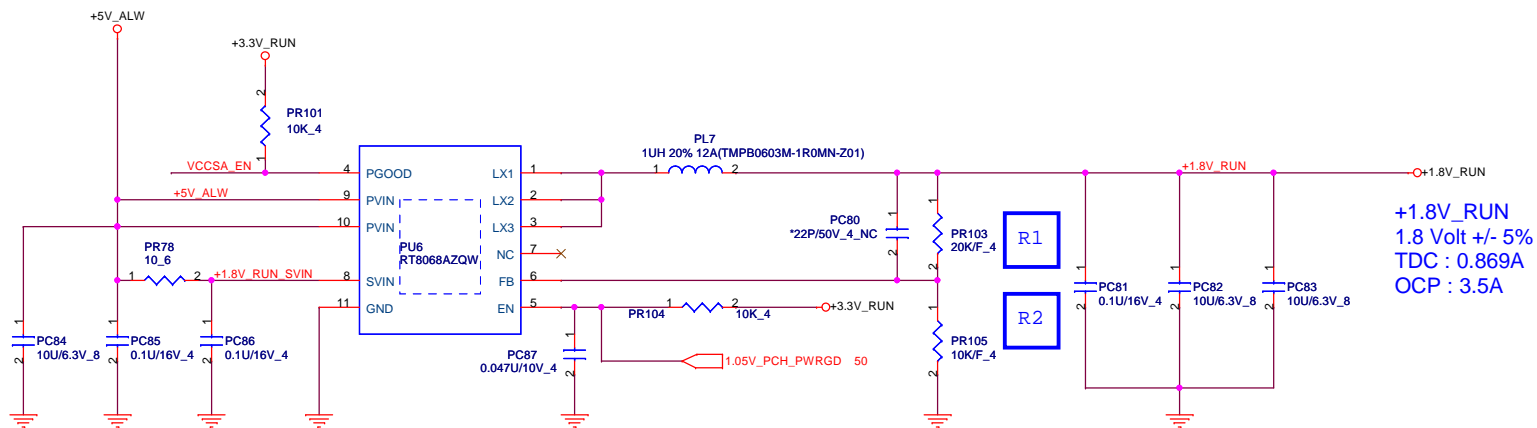
PROJECT : R08

Size	Document Number	Rev
	+1.05V_PCH / VTT (RT8240BGQW)	1A
Date:	Monday, February 13, 2012	Sheet 50 of 55

Need confirm
with EE or not
have pull high
resistor for PG.



VCCSA_VID1	VCCSA_VID0	VCCSA_CORE
Low	Low	0.9V
High	Low	0.8V
Low	High	0.725V
High	High	0.675V



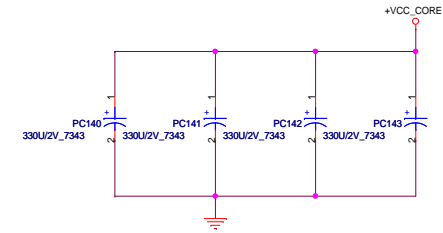
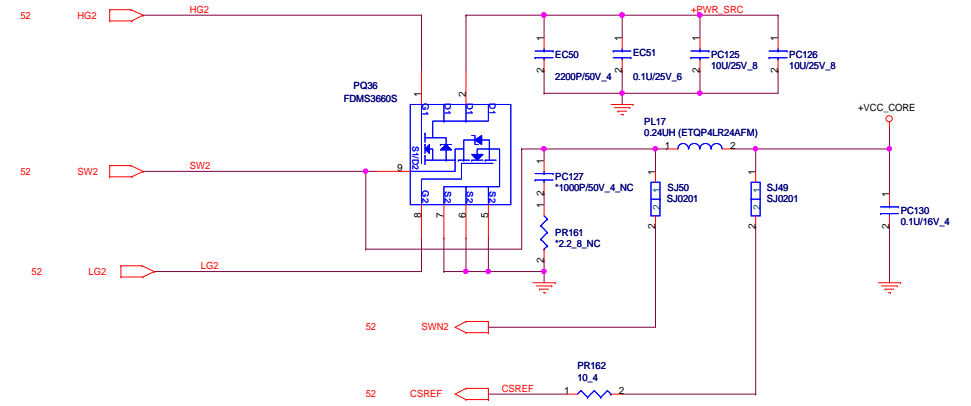
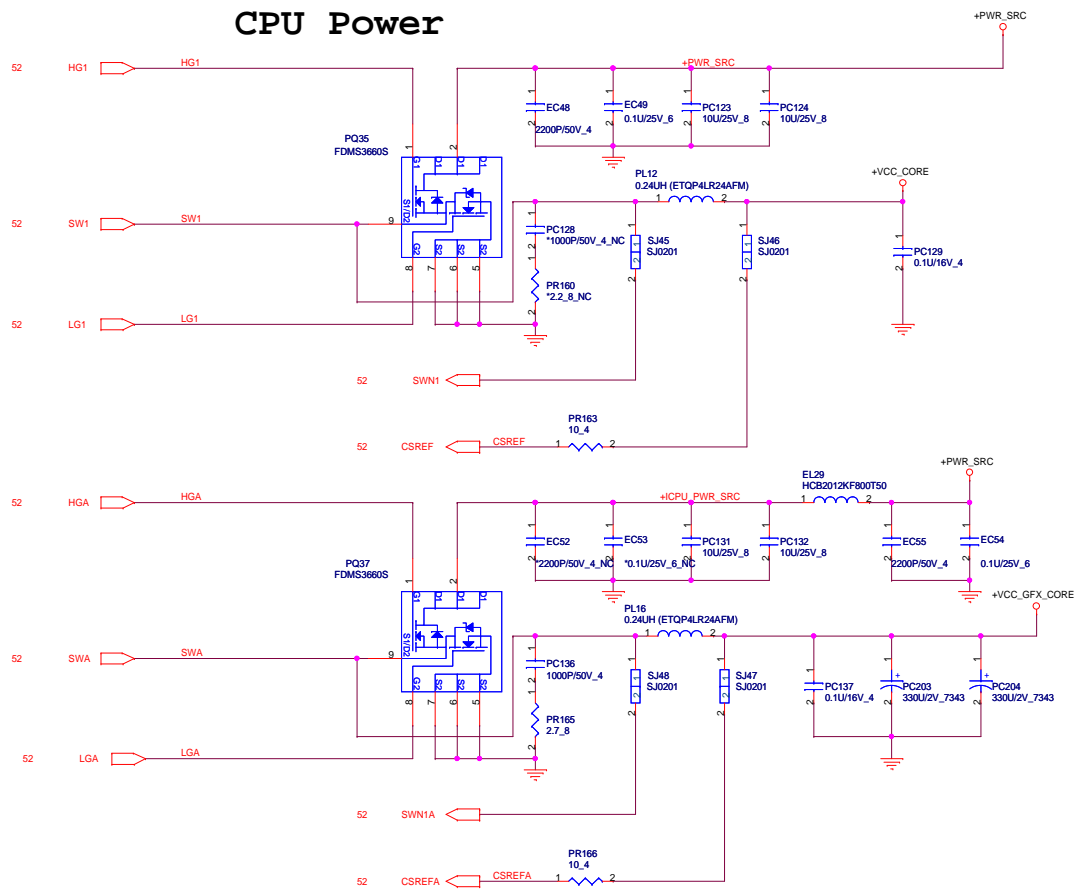
$$VOUT = 0.6(1+R1/R2)$$



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CPU Power



Adapter type	65W	90W
ADAPT_TRIP_SET	0	1
SETTING CURRENT	3.7A	5.6A

